

Commercial DT / M4.1 Chassis System

Project name: vHulk

SCH Ver: -1

PCB Number: 14065-1

PCB BOARD SIZE

4 Layer / 244 mm x 244 mm

PAGE	TITLE
01	COVER PAGE
02	BLOCK DIAGRAM
03	CPU (PCIE/DMI)
04	CPU (CFG/CLOCK/PM)
05	CPU (DDR_CHA)
06	CPU (DDR_CHB)
07	CPU (DDI/EDP)
08	CPU (CPU Power)
09	CPU (VSS)
10	CPU (Power CAP)
11	DDR DIMM_2
12	DDR DIMM_1
13	DDR DIMM_4
14	DDR DIMM_3
15	PCH (SPI/UART/I2C)
16	PCH (DMI/PCI-E/USB)DDI GP
17	PCH (PCI-E/SATA)
18	PCH (CLOCK/CL)
19	PCH (USB/ESPI)
20	PCH(GPIO/CPU/SMBUS/IHDA/JTAG)
21	PCH (POWER1)
22	PCH (POWER2)_PCH Strap
23	PCH Power CAP
24	SIO ITE8733
25	Flash&RTC
26	Thermal&FAN
27	Audio Codec ALC662
28	AMP_(R)
29	Audio IO Front
30	Audio IO Rear
31	LAN RTL8111EPV
32	RJ45&Transformer
33	Card Reader_(R)
34	USB Charger_(R)
35	USB Redrive_(R)
36	USB20_REAR PORT
37	USB20_FRONT HEADER
38	USB30_REAR PORT
39	USB30_FRONT HEADER
40	Power Plane EN Sequence
41	Dual Power
42	Switch power
43	ATX(BATT Conn)
44	Power Sequence(DDR4)
45	DCDC-3D3V&5V
46	VCORE & V_GT IC(NCP81203)
47	VCORE OUTPUT (NCP81151)
48	V_GT OUTPUT(NCP81151)
49	5V &3.3V(RT8243A)
50	DDR_PWR (RT8207M)
51	PCH_1P0V(RT8237C)
52	VCC_SA(NCP5230M)
53	VCC_IO(RT8237C)
54	LDO_1P5V_1P8V_2P5V

PAGE	TITLE
55	DVI-D
56	DP2
57	DP1
58	DVI/CRT
59	PCI bridge
60	HDD/ODD
61	Mini card-WLAN
62	Mini card-SSD (R)
63	Mini card-NGFF
64	Front board
65	Others
66	IO Board_(R)
67	COM
68	Debug
69	LPT
70	G sensor_(R)
71	Thunderbolt_(R)
72	Thunderbolt_(R)
73	Thunderbolt_(R)
74	Thunderbolt_(R)
75	Thunderbolt_(R)
76	GPU_(R)
77	GPU_(R)
78	GPU_(R)
79	GPU_(R)
80	GPU_(R)
81	GPU VRAM 1&2_(R)
82	GPU VRAM 3&4_(R)
83	GPU VRAM 5&6_(R)
84	GPU VRAM 7&8_(R)
85	GPU CORE_(R)
86	GPU discrete power_(R)
87	GPU Switch_(R)
88	GPU Switch_(R)
89	GPU others_(R)
90	NFC_(R)
91	TPM
92	PS2
93	Express Card
94	Smart Card
95	Scalar_(R)
96	MCU_(R)
97	Inter LAN
98	LAN Switch_(R)
99	XDP&ITP
100	Table of Content
101	GPIO table
102	POWER SEQUENCE
103	Power Block Diagram
104	SMBUS table
105	CLOCK MAP
106	RESET Flow CHART
107	Change History

Jumper SETTING

CMOS1	1-2 Short	With Jumper to Clear CMOS
WP1	1-2 Short	With Jumper to enable WP
OBR1	1-2 Open	Without Jumper to recovery
MECLR1	1-2 Short	With Jumper to enable ME

BOM Configuration

(R_) : unmount
(E_) : SATA Express
(Q_) : Q170
(B_) : B150
(D_) : VGA
(W_) : For WST/FXC MB
(T_) : TPM on board
(S_) : For ECS MB
(H_) : TPM header

Key IC

CPU1	Intel CPU Skylake S 65W
PCH1	Intel PCH Q170/B150
U7901	ITE SIO IT8733F-DX
U2701	RealTek Audio Codec ALC662-VD
U3	Realtek LAN RTL8111EPV-CG
TPM1	NuvoTon TPM NPCT650AAAWX
U72	INTEL LAN I219LM I219
U54	ITE PCI Bridge IC IT8893E
U6506	Realtek converter RTD2168-CG


Header

SPK1	21.63415.204
AUDF1	21.62895.205
FANC1	21.60626.104
FANS1	21.60626.104
CMOS1	21.61445.103
OBR1	21.60909.102
WP1	21.61445.103
PCHDR1	021.60235.0204
LPT1	021.60217.0213
COM1	21.62884.205
TPMH1	21.62900.210
CSOPN1	21.62874.102
MECLR1	21.61445.103

Power sates

	Name	G3	EUP	S5	S4	S3	S0
+12V	12V_S0 12V_CPU_S0						O
-12V	-12V_S0						O
5V	ATX_5VSB +5V_AUX1 +5V_AUX2 5V_USB20_RJUSB2 5V_USB30P1 5V_USB30P2 5V_USB30H1 5V_USB20P1 5V_USB20_RJUSB1 5V_USB20H2 5V_USB20H1 5V_USB30H2 5V_S0 5V_DVI		O	O	O	O	O
3.3V	ATX_3.3VSB 3P3V_LAN 3P3V_S5 3D3V_VCCPGPPA_Sx 3D3V_1D8V_PCHSPI_Sx 3D3V_DVDDIO_AUDIO DVDD_IO 3D3V_S0 3D3V_RTD2168		O	O	O	O	O
3.0V	3V_VBAT1_G3 3V_VRTC_G3 3D3V_VCCPRTC	O	O	O	O	O	O
2.5V	2D5V_VFP				O	O	O
1.2V	VDDQ				O	O	O
DIMM	DDR_VTT 1D0V_S5 1V_VCCF24_Sx 1V_VCCAMPHYPLL_Sx 1V_VCCAPLL_Sx			O	O	O	O
PCH	VCC_CORE GFX_CORE VCC_SA VCC_IO 1V_VCCST_VCCPLL_S3						O

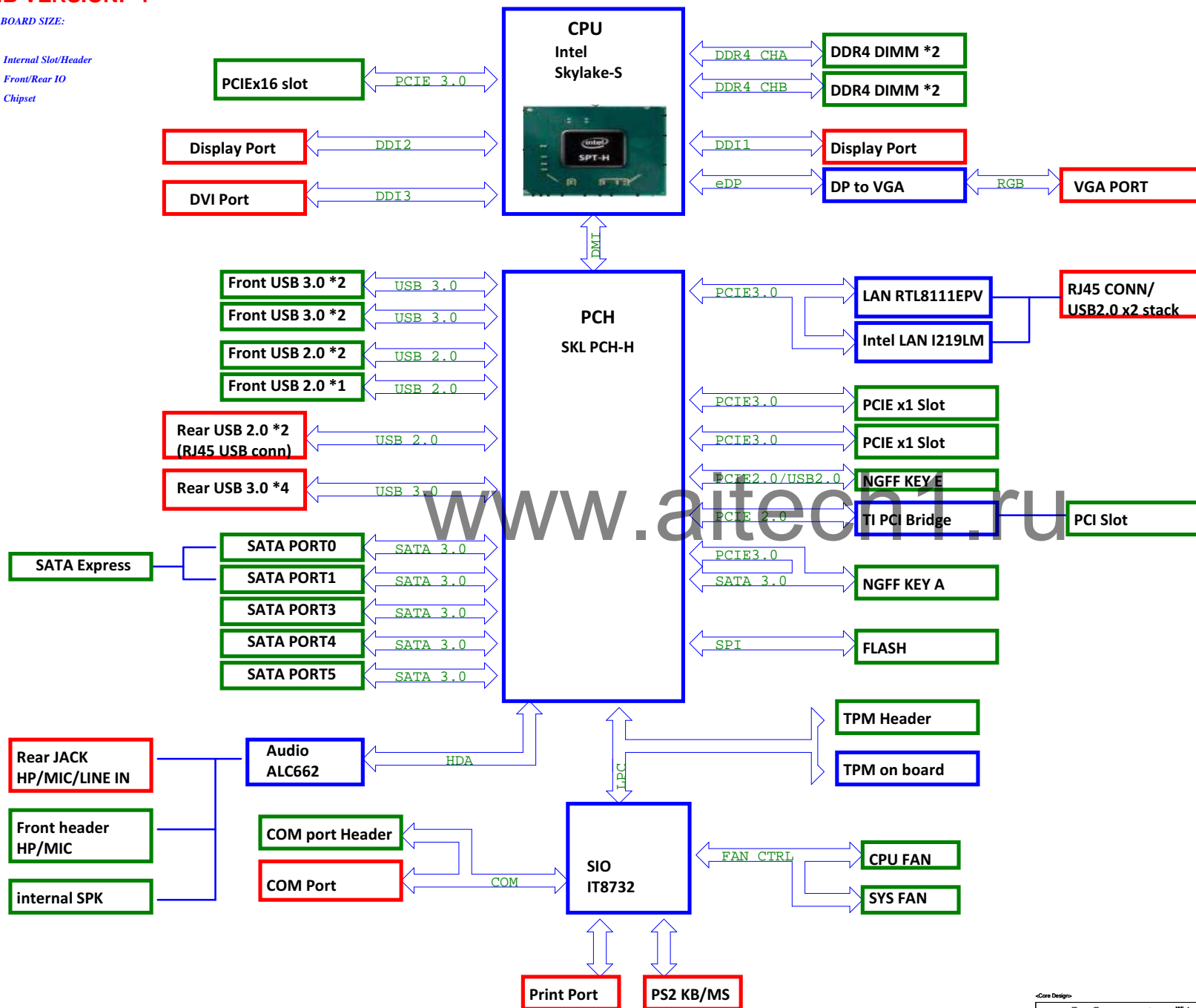
<Core Design>

		Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsinchu, Taipei, Taiwan
Title: COVER PAGE		
Size: C	Document Number: vHulk	Rev: -1
Date: Wednesday, September 23, 2015	Sheet: 1 of 107	

PROJECT NAME: vHULK
MB VERSION: -1

PCB BOARD SIZE:

- Internal Slot/Header
- Front/Rear IO
- Chipset



<Core Design>

wistron

Wistron Incorporated
21F, 8B, Sec. 1, Hsin Tai Wu Rd
Hsinchu, Taipei Hsin

Block Diagram

Customer: vHulk

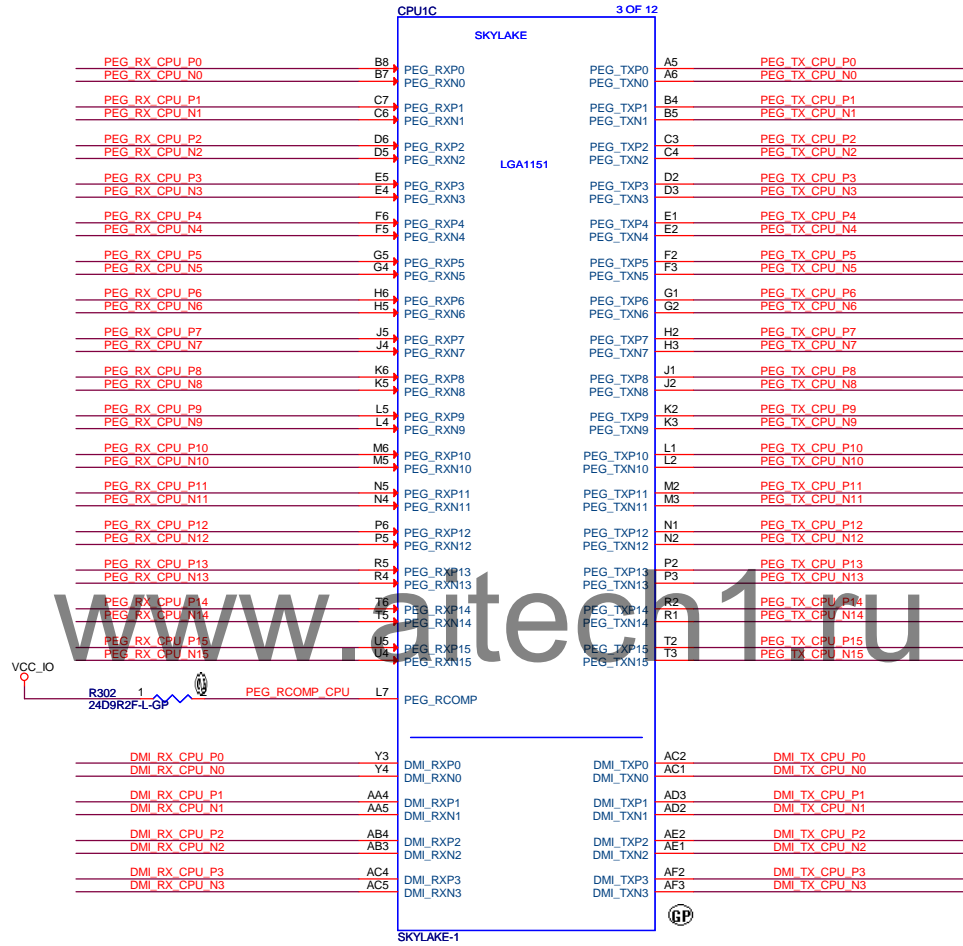
Date: Wednesday, September 23, 2015 Sheet 2 of 107

PEG

93 PEG_TX_CPU_P[0..15] <<<<
93 PEG_TX_CPU_N[0..15] <<<<
93 PEG_RX_CPU_P[0..15] >>>>
93 PEG_RX_CPU_N[0..15] >>>>

DMI

16 DMI_RX_CPU_P[0..3] <<<<
16 DMI_RX_CPU_N[0..3] <<<<
16 DMI_TX_CPU_P[0..3] >>>>
16 DMI_TX_CPU_N[0..3] >>>>



FOXCONN: 062.10015.0081
LOTES: 062.10015.0111

<Core Design>

wistron		Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title CPU(PCIE/DMI)			
Size Custom	Document Number vHulk		Rev -1
Date: Wednesday, September 23, 2015		Sheet 3	of 107

XDP_PCODEBUG<3> >>
 CFG0_15] >>
 SKL_PCUSTB_0_DP >>
 SKL_PCUSTB_0_DN >>
 SKL_PCUSTB_1_DP >>
 SKL_PCUSTB_1_DN >>
 BPM_CPU_N0 >>
 BPM_CPU_N1 >>
 H_TDO >>
 H_TDI >>
 H_TMS >>
 H_TCK >>
 H_TRST_N >>
 H_PREQ_N >>
 H_PRDY_N >>

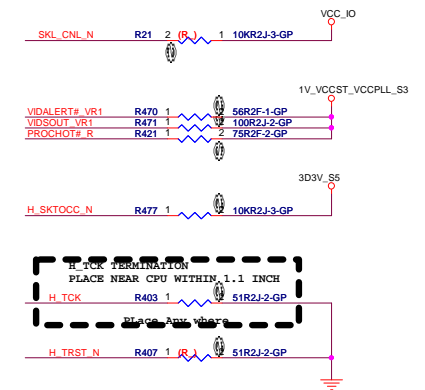
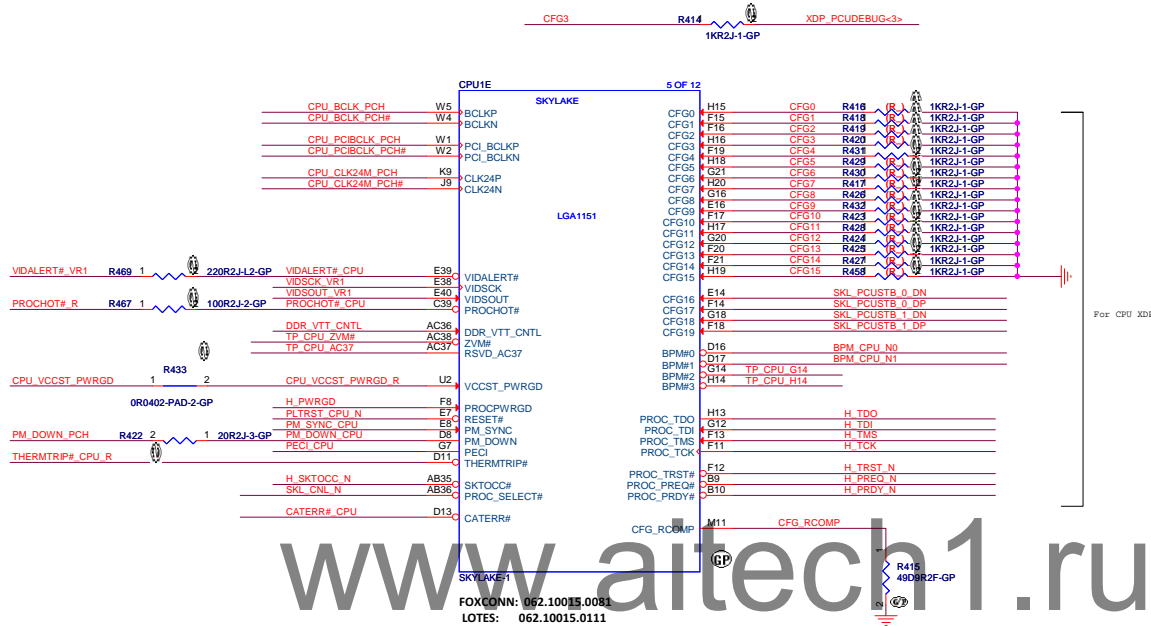
```
46  VIDSCK_VR1      >>—
46  VIDSOUT_VR1     >>—
46  VIDALERT#_VR1  >>—
```

```

18 CPU_BCLK_PCH
18 CPU_BCLK_PCH#
18 CPU_PCIBCLK_PCH
18 CPU_PCIBCLK_PCH#
18 CPU_CLK24M_PCH
18 CPU_CLK24M_PCH#

```

46	PROCHOT#_R	>>
44	DDR_VTT_CNTL	>>
40	CPU_VCCST_PWGRD	>>
20	H_PWRGD	>>
17	PLTRST_CPU_N	>>
17	PM_SYNC_CPU	>>
17	PM_DOWN_PCH	<<
17,24	PECL_CPU	<<
17	THERMTRIP#_CPU_R	<<
16	H_SKT0CC_N	<<



- **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted:
 - 1 = (Default) Normal Operation;
 - 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
 - 1 = Normal operation
 - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
 - 1 = Disabled.
 - 0 = Enabled.
- **CFG[6:5]:** PCI Express* Bifurcation
 - 00 = 1 x8, 2 x4 PCI Express*
 - 01 = reserved
 - 10 = 2 x8 PCI Express*
 - 11 = 1 x16 PCI Express*
- **CFG[7]:** PEG Training:
 - 1 = (default) PEG Train immediately following RESET# de assertion.
 - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.

12,14 M_DATA_A[0..63] << >>
12,14 M_A_A[0..16] << >>
12,14 M_A_DQS_DN[0..7] << >>
12,14 M_A_DQS_DP[0..7] << >>

14 M_A_CLK0 << >>
14 M_A_CLK#0 << >>
14 M_A_CLK1 << >>
14 M_A_CLK#1 << >>
12 M_A_CLK2 << >>
12 M_A_CLK#2 << >>
12 M_A_CLK3 << >>
12 M_A_CLK#3 << >>

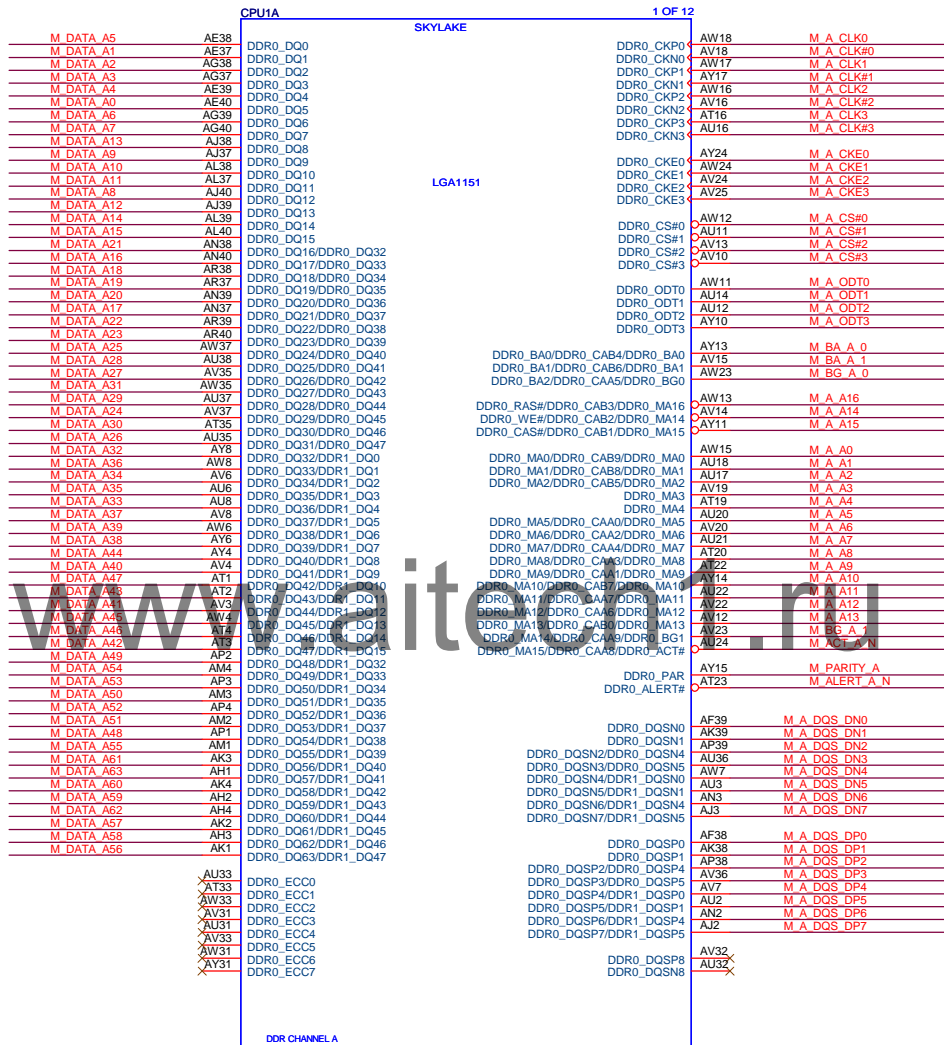
14 M_A_CKE0 << >>
14 M_A_CKE1 << >>
12 M_A_CKE2 << >>
12 M_A_CKE3 << >>

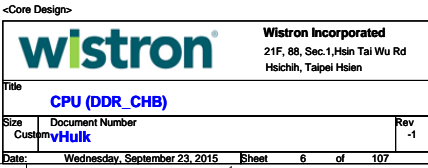
14 M_A_CS#0 << >>
14 M_A_CS#1 << >>
12 M_A_CS#2 << >>
12 M_A_CS#3 << >>

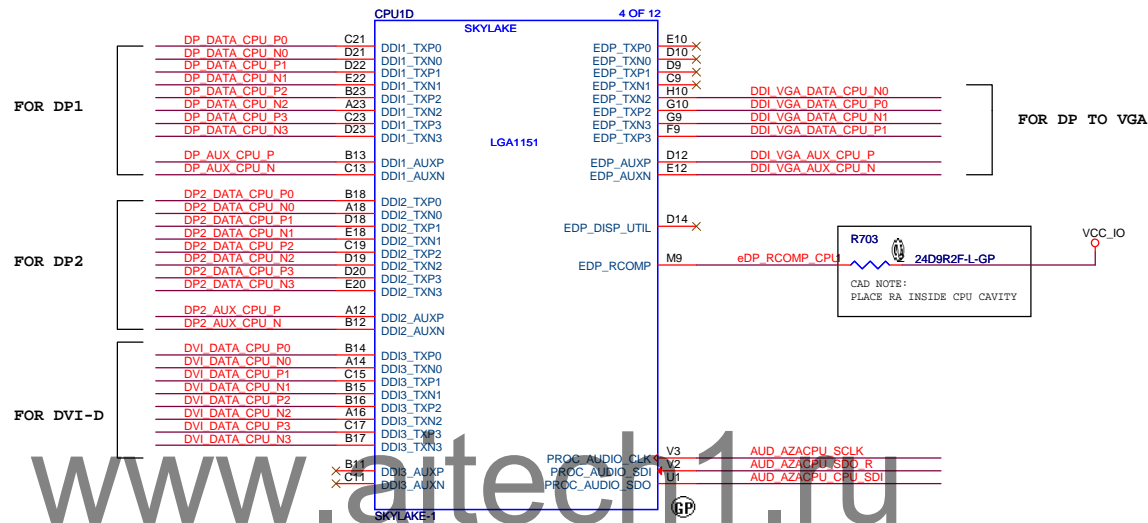
14 M_A_ODT0 << >>
14 M_A_ODT1 << >>
12 M_A_ODT2 << >>
12 M_A_ODT3 << >>

12,14 M_BA_A_1 << >>
12,14 M_BA_A_0 << >>
12,14 M_BG_A_1 << >>
12,14 M_BG_A_0 << >>

12,14 M_PARITY_A << >>
12,14 M_ALERT_A_N << >>
12,14 M_ACT_A_N << >>







VBIOS set as DP

Note:

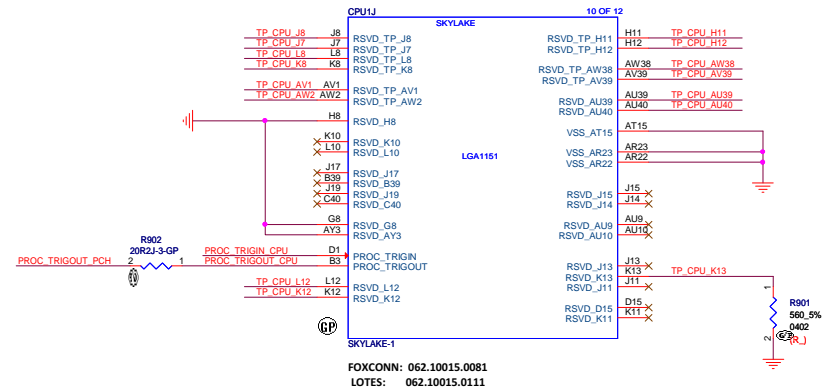
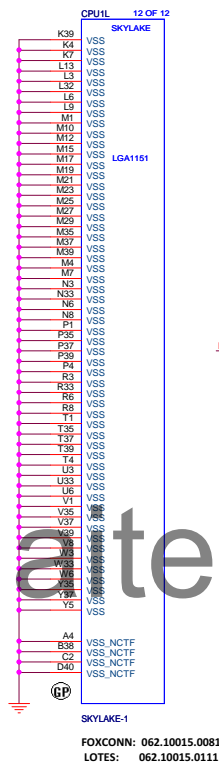
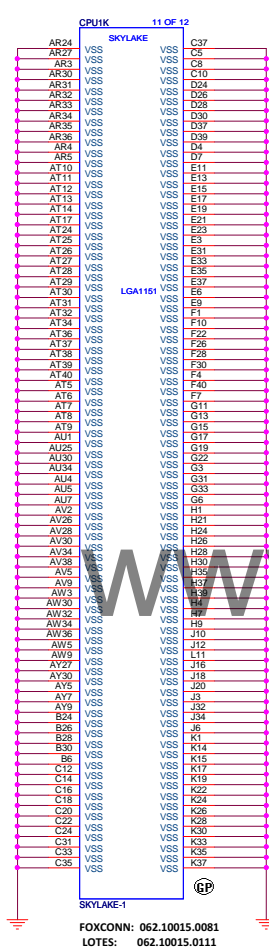
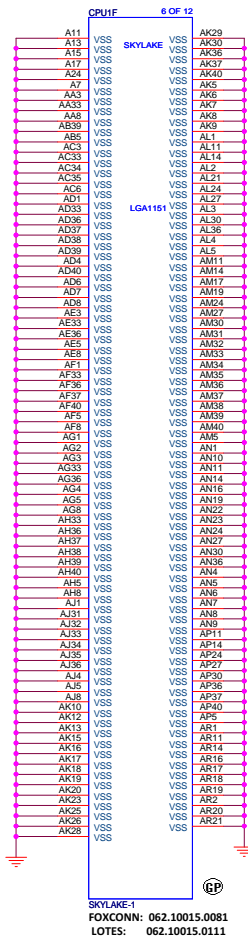
1. When using eDP bifurcation:
 - x2 eDP lanes for eDP panel (eDP_TXP[0:1], eDP_TXN[0:1])
 - x2 lanes for DP (eDP_TXP[2:3], eDP_TXN[2:3])

FOXCONN: 062.10015.0081
 LOTES: 062.10015.0111

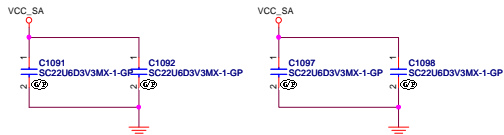
<Core Design>



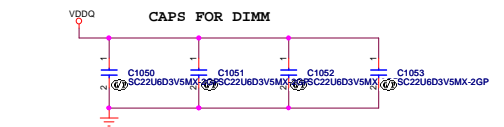
21 PROC_TRIGIN_CPU >>>
21 PROC_TRIGOUT_PCH <<<



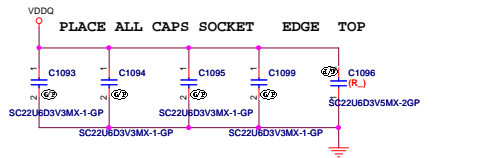
PLACE ALL CAPS INSIDE CPU SOCKET CAVITY ON TOPSIDE



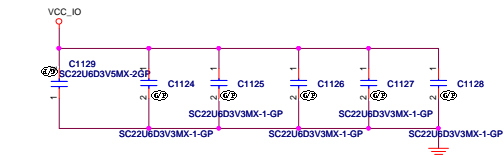
CAPS FOR DIMM



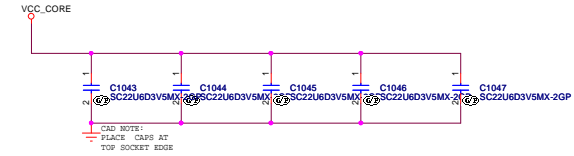
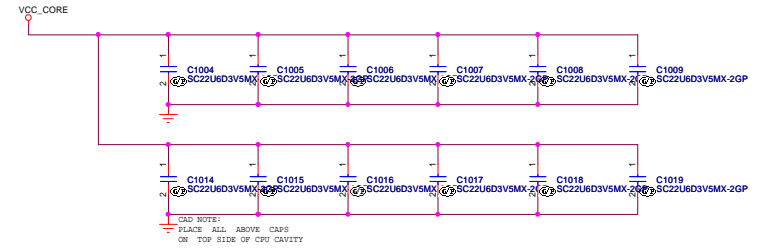
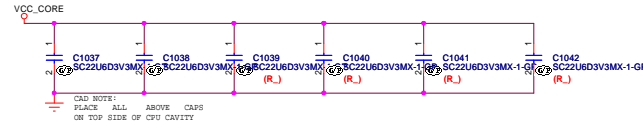
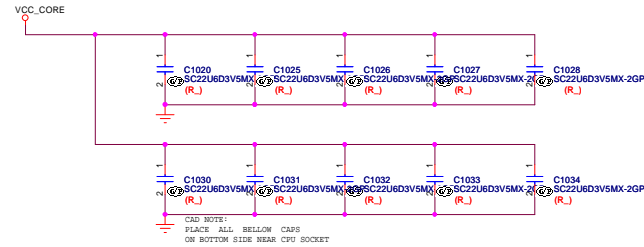
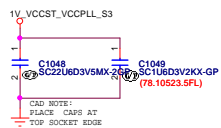
PLACE ALL CAPS SOCKET EDGE TOP



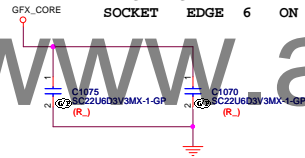
PLACE ALL CAPS INSIDE CPU SOCKET CAVITY ON TOPSIDE



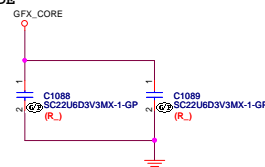
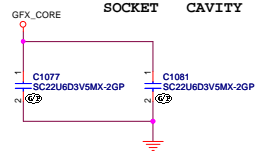
PLACE ALL CAPS OUTSIDE CPU SOCKET CAVITY ON TOPSIDE



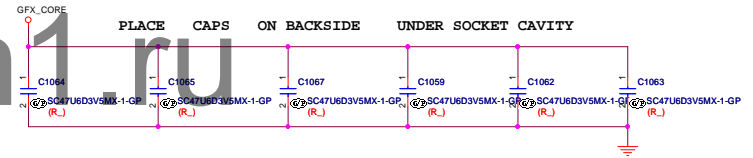
PLACE CAPS AT SOCKET EDGE 6 ON TOP & 6 ON BOTTOM



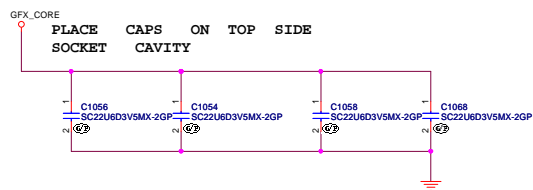
PLACE CAPS ON TOP SIDE SOCKET CAVITY



PLACE CAPS ON BACKSIDE UNDER SOCKET CAVITY

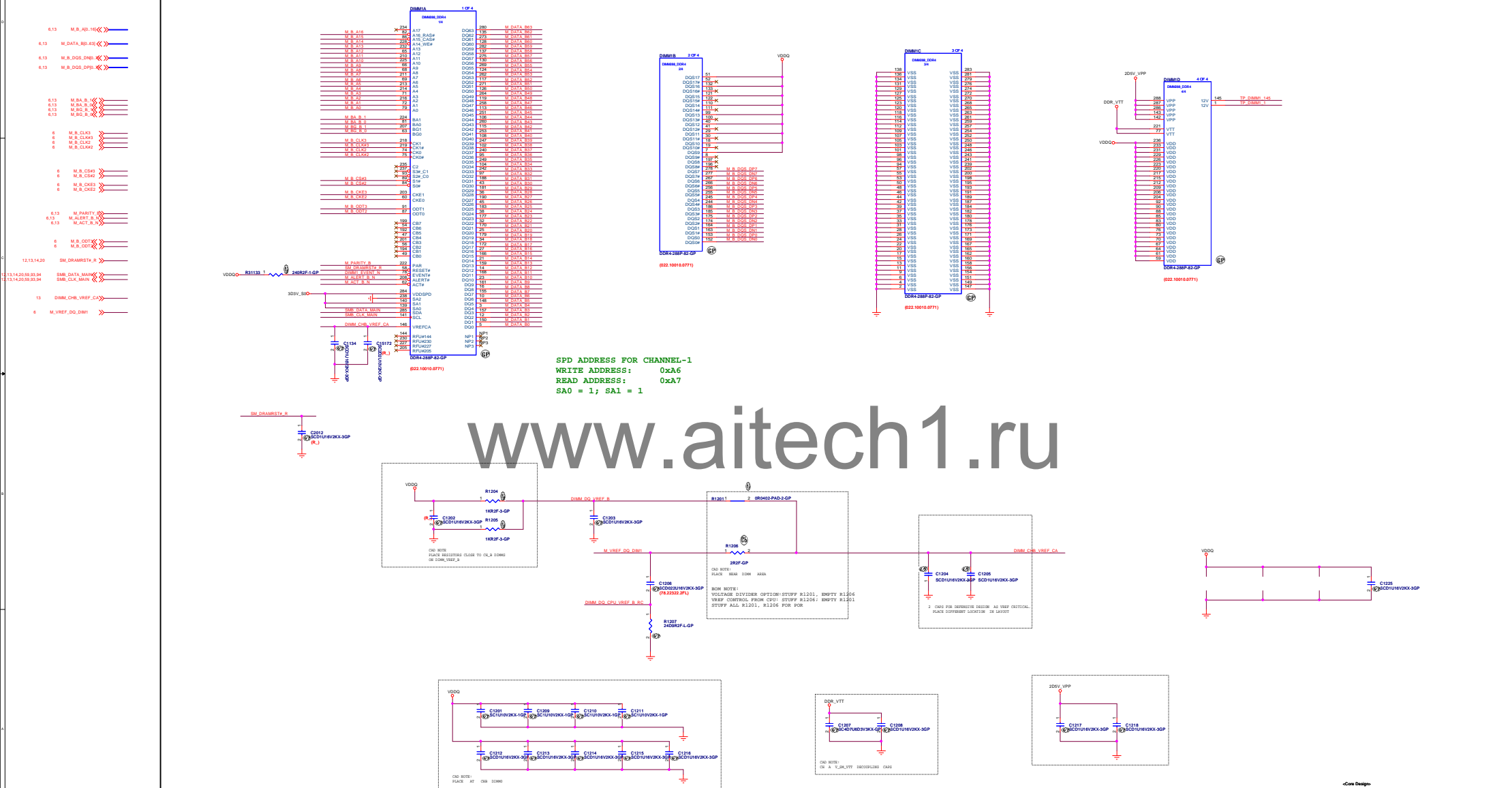


PLACE CAPS ON TOP SIDE SOCKET CAVITY



<Core Design>

CHANNEL B -- DIMM1



CHANNEL A -- DIMM1

5.14 M_A_A0[16] <<>
5.14 M_DATA_A0[63] <<>
5.14 M_A_DQS_DPB[8] <<>
5.14 M_A_DQS_DNB[8] <<>

5.14 M_BA_A[1] <<>
5.14 M_BA_A[2] <<>
5.14 M_BA_A[3] <<>

5 M_A_CLK3 <<>
5 M_A_CLK4 <<>
5 M_A_CLK2 <<>
5 M_A_CLK42 <<>

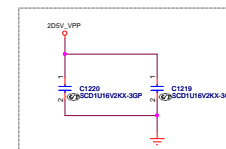
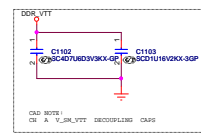
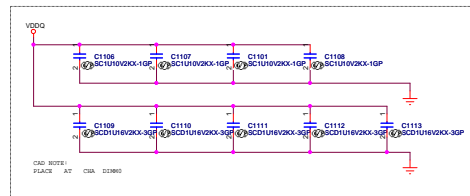
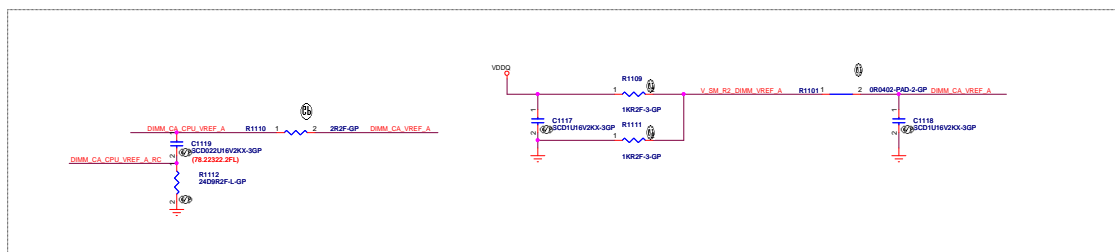
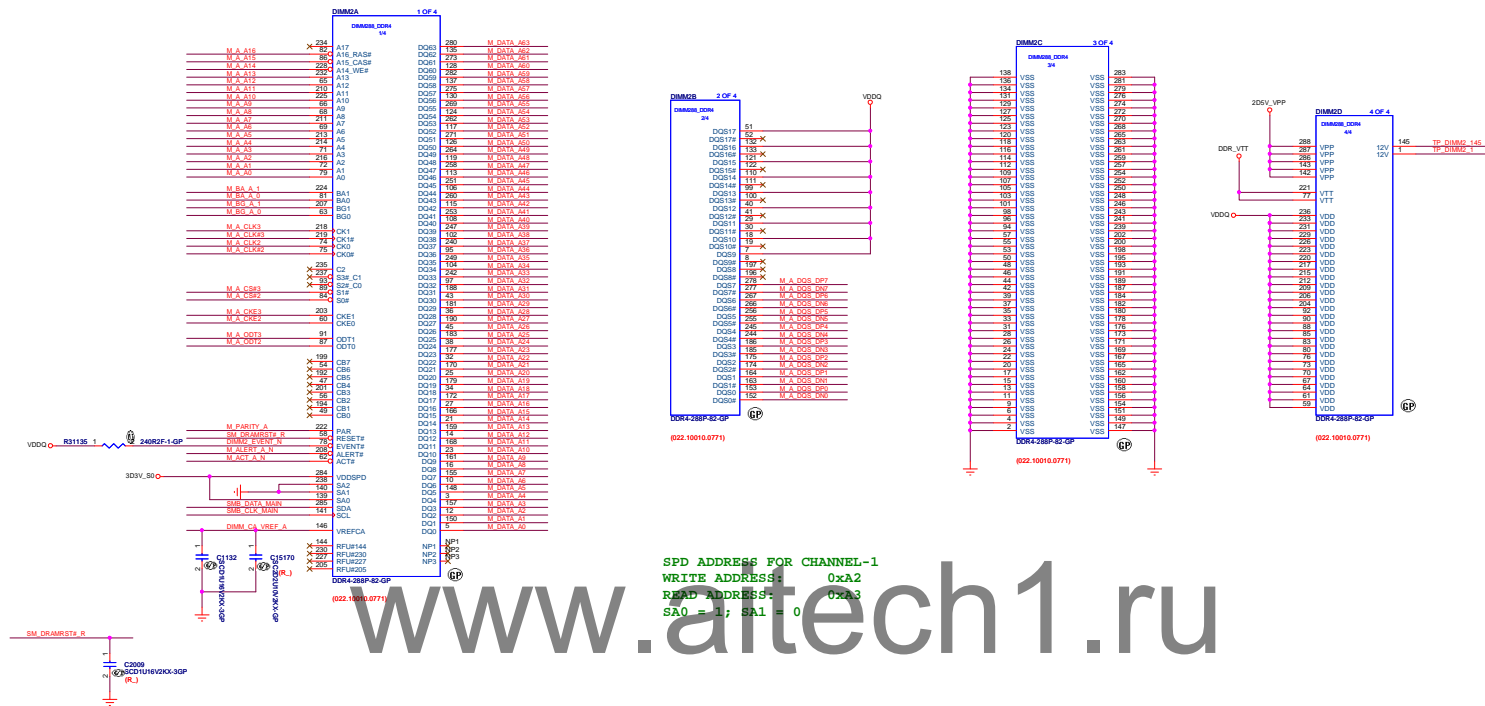
5 M_A_ODT3 <<>
5 M_A_ODT2 <<>

5 M_A_CS0 <<>
5 M_A_CS4 <<>
5 M_A_CS3 <<>
5 M_A_CS2 <<>
5 M_A_CS1 <<>
5 M_A_CS5 <<>

5.14 M_PARITY <<>
5.14 M_ALERT_A[8] <<>
5.14 M_ALERT_A[7] <<>
5.14 M_ALERT_A[6] <<>
5.14 M_ALERT_A[5] <<>
5.14 M_ALERT_A[4] <<>
5.14 M_ALERT_A[3] <<>
5.14 M_ALERT_A[2] <<>
5.14 M_ALERT_A[1] <<>
5.14 M_ALERT_A[0] <<>

11,13,14,20 SM_DRAMSTB_R <<>
11,13,14,20,59,93,94 SMB_DATA_MAIN <<>
11,13,14,20,59,93,94 SMB_CLK_MAIN <<>

14 DIMM_CA_VREF_A <<>
0 DIMM_CA_VREF_A <<>



©2015 Wistron

wistron

Wistron Incorporated
21F, 88, Sec.1 Hsin Tai Wu Rd
Hsinchu, Taipei, Taiwan

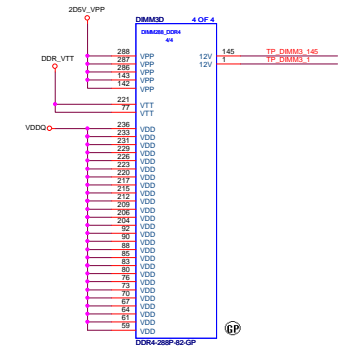
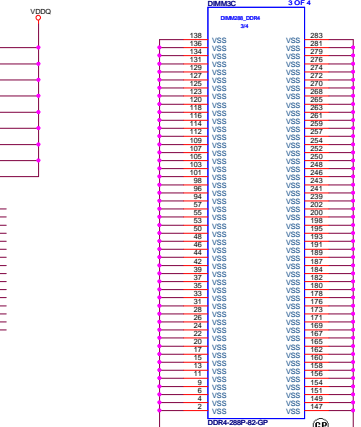
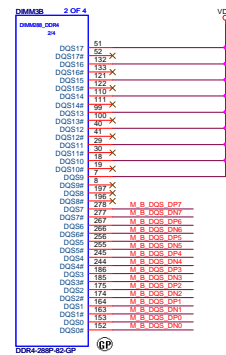
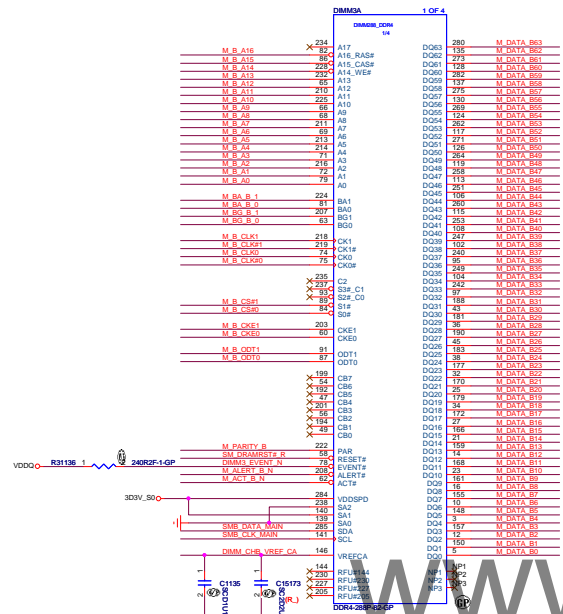
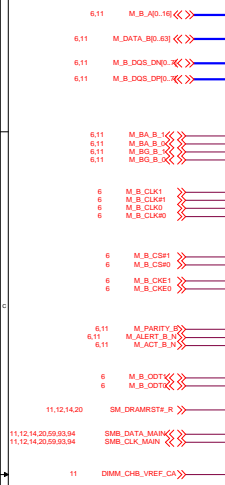
Doc: DDR-DIMM_2

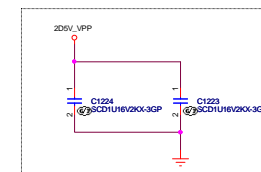
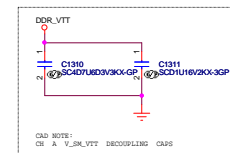
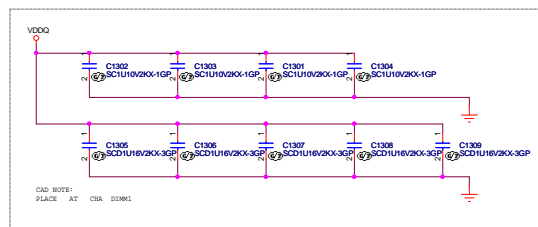
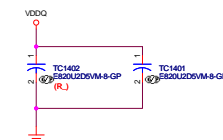
Rev: 1

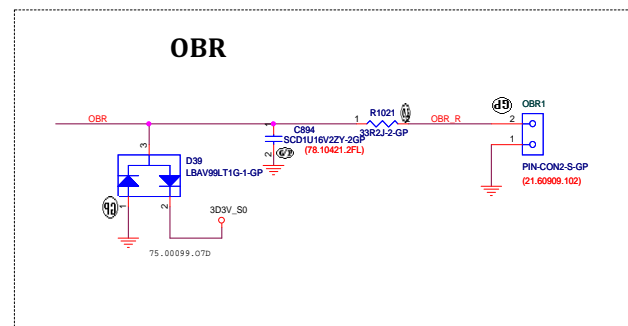
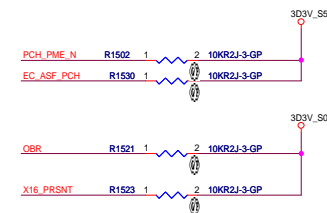
Date: Wednesday, September 23, 2015

Page: 12 of 107

CHANNEL B -- DIMM0







DMI

3 DMI_TX_CPU_N0_3
3 DMI_TX_CPU_P0_3
3 DMI_RX_CPU_N0_3
3 DMI_RX_CPU_P0_3

USB3.0

39 USB30_RX_PCH_N7
39 USB30_RX_PCH_P7
39 USB30_TX_PCH_N7
39 USB30_TX_PCH_P7
39 USB30_TX_PCH_N8
39 USB30_TX_PCH_P8
39 USB30_RX_PCH_N8
39 USB30_RX_PCH_P8

PCIE

31,97 PCIE_RX_LAN_N5
31,97 PCIE_RX_LAN_P5
31,97 PCIE_TX_LAN_N5
31,97 PCIE_TX_LAN_P5

61 PCIE_RX_PCH_N6
61 PCIE_RX_PCH_P6
61 PCIE_TX_CON_N6
61 PCIE_TX_CON_P6

59 PCIE_RX_PCH_N7
59 PCIE_RX_PCH_P7
59 PCIE_TX_CON_N7
59 PCIE_TX_CON_P7

94 PCIE_RX_PCH_N8
94 PCIE_RX_PCH_P8
94 PCIE_TX_CON_N8
94 PCIE_TX_CON_P8

USB2.0

38 USB_PCH_PN1
38 USB_PCH_PN2
38 USB_PCH_PP2
38 USB_PCH_PN3
38 USB_PCH_PN4
38 USB_PCH_PN5
38 USB_PCH_PP5
38 USB_PCH_PN6
38 USB_PCH_PP6
37 USB_PCH_PN7
37 USB_PCH_PP7
37 USB_PCH_PN8
37 USB_PCH_PP8
37 USB_PCH_PN9
37 USB_PCH_PP9
36 USB_PCH_PN10
36 USB_PCH_PP10
36 USB_PCH_PN11
36 USB_PCH_PP11
61 USB_PCH_PN12
61 USB_PCH_PP12
39 USB_PCH_PN13
39 USB_PCH_PP13
39 USB_PCH_PN14
39 USB_PCH_PP14

USB OC CTRL

42 USB30_OC_H1#
42 USB30_OC_P1#
42 USB30_OC_P2#
22 VISACH2_D3
42 USB30_OC_P1#
42 USB30_OC_P2#
42 USB30_OC_H2#

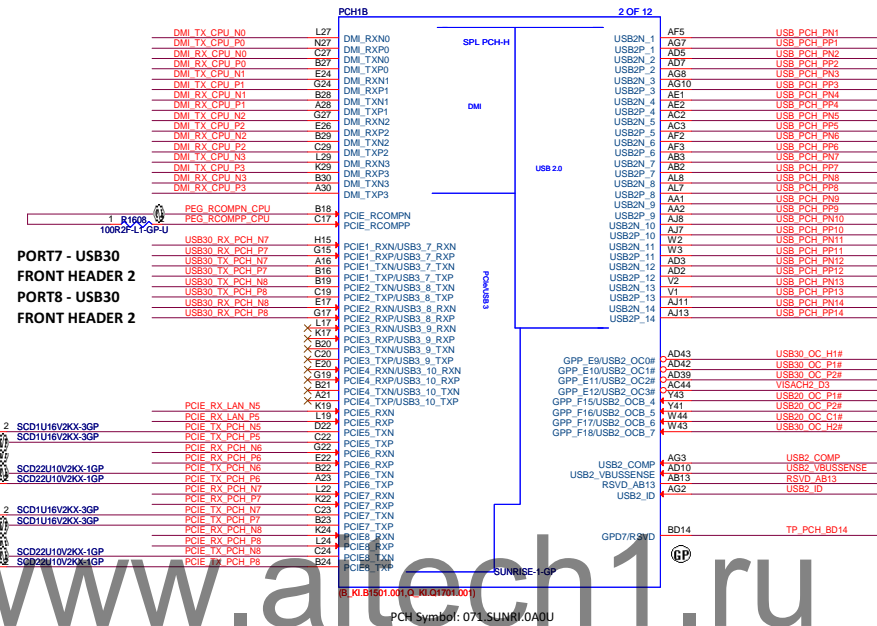
DISPLAY CTRL

57 DP_HPD_PCH
56 DP2_HPD_PCH
57 DVI_DET_PCH
58 CRT_HPD_PCH

56 DP2_CTRLCLK_PCH
56 DP2_CTRLDATA_PCH
57 DP_CTRLCLK_PCH
57 DP_CTRLDATA_PCH
55 DVI_CLK_PCH
55 DVI_DATA_PCH

GPIO

4 H_SKT0CC_N



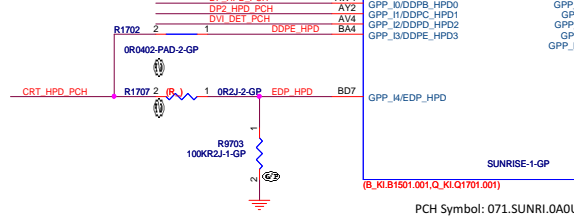
USB Table

Pair	Device
1	USB3.0 Ext. port 1 (Rear)
2	USB3.0 Ext. port 2 (Rear)
3	USB3.0 Ext. port 3 (Rear)
4	USB3.0 Ext. port 4 (Rear)
5	USB3.0 Ext. Header (Front)
6	USB3.0 Ext. Header (Front)
7	USB2.0 Ext. Header (Front)
8	CR Ext. Header (Front)
9	USB2.0 Ext. Header (Front)
10	RJ45+USB Dual port
11	RJ45+USB Dual port
12	NGFFE1
13	USB3.0 Ext.Header (Front) for Q170 bom option
14	USB3.0 Ext.Header (Front) for Q170 bom option

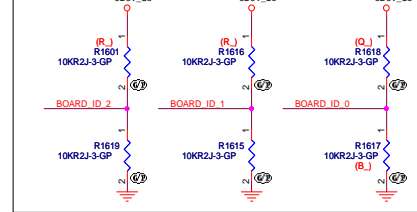
FOR LAN
FOR NGFFE1
PCIE to PCI Bridge
FOR PCIE2

Close to CONN
PCIE_TX_LAN_N5
PCIE_TX_LAN_P5
PCIE_TX_LAN_N6
PCIE_TX_LAN_P6
PCIE_TX_CON_N6
PCIE_TX_CON_P6
PCIE_TX_CON_N7
PCIE_TX_CON_P7
PCIE_TX_CON_N8
PCIE_TX_CON_P8

2014/9/9
DDI1 to DP1
DDI2 to DP2
DDI3 to DVI



BOARD ID



Board_ID_0
pull high for Q170
pull low for B150

<Core Design>

wistron
Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsinchu, Taipei, Taiwan

Title: **PCB (DMI/PCI-E/USB)**
Size: **C**
Document Number: **vHulk**
Date: **Wednesday, September 23, 2015**
Sheet: **16** of **107**

CL BUS

61 WLAN_CLK_PCH <<
61 WLAN_DAT_PCH <<
61 WLAN_RST_PCH <<

PCIE

94 PCIE_TX_CON_P11 <<
94 PCIE_TX_CON_N11 <<
94 PCIE_RX_PCH_P11 <<
94 PCIE_RX_PCH_N11 <<

SATA PORT

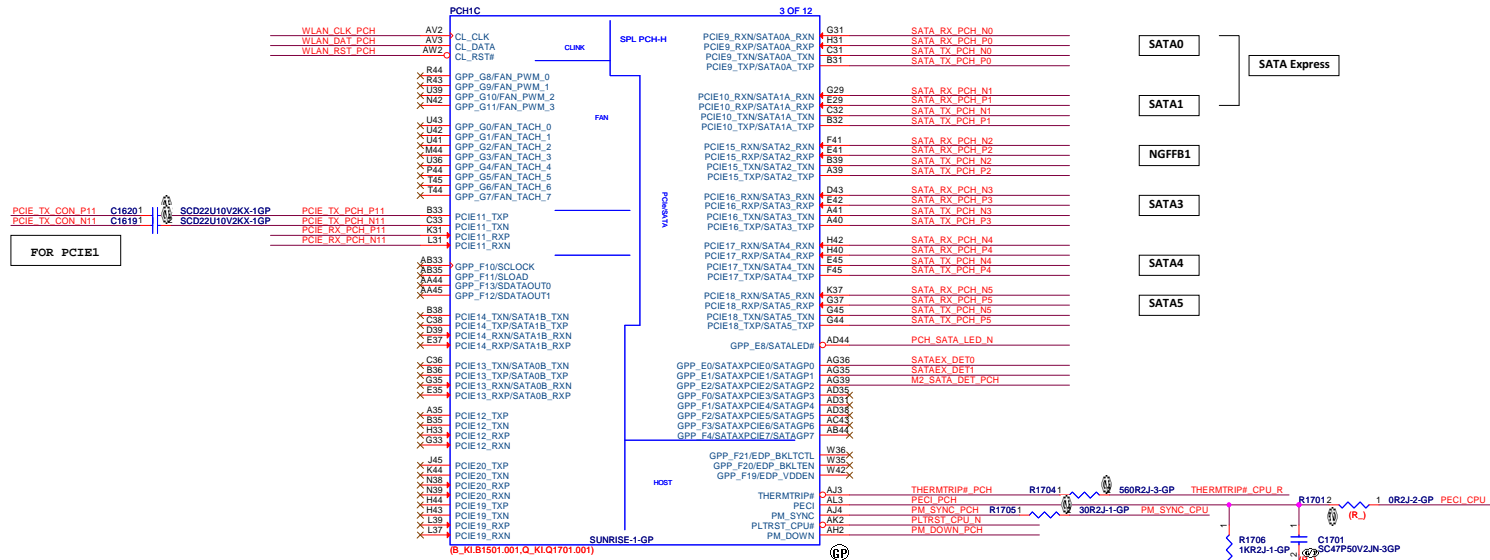
60 SATA_RX_PCH_N0 <<
60 SATA_RX_PCH_P0 <<
60 SATA_TX_PCH_N0 <<
60 SATA_TX_PCH_P0 <<
60 SATA_RX_PCH_N1 <<
60 SATA_RX_PCH_P1 <<
60 SATA_TX_PCH_N1 <<
60 SATA_TX_PCH_P1 <<
63 SATA_RX_PCH_N2 <<
63 SATA_RX_PCH_P2 <<
63 SATA_TX_PCH_N2 <<
63 SATA_TX_PCH_P2 <<
60 SATA_RX_PCH_N3 <<
60 SATA_RX_PCH_P3 <<
60 SATA_TX_PCH_N3 <<
60 SATA_TX_PCH_P3 <<
60 SATA_RX_PCH_N4 <<
60 SATA_RX_PCH_P4 <<
60 SATA_TX_PCH_N4 <<
60 SATA_TX_PCH_P4 <<
60 SATA_RX_PCH_N5 <<
60 SATA_RX_PCH_P5 <<
60 SATA_TX_PCH_N5 <<
60 SATA_TX_PCH_P5 <<

SATA DET

60 SATAEX_DET0 >>
60 SATAEX_DET1 >>
63 M2_SATA_DET_PCH >>
64 PCH_SATA_LED_N <<

HOST

4 THERMTRIP#_CPU_R >>
4,24 PECL_CPU <<
4 PLTRST_CPU_N <<
4 PM_DOWN_PCH >>
4 PM_SYNC_CPU <<



www.aitech1.ru



```

4    CPU_CLK24M_PCH
4    CPU_CLK24M_PCH#

4    CPU_BCLK_PCH
4    CPU_BCLK_PCH#

```

63	PEG_CLKREQ0_M2#	
61	PEG_CLKREQ1_WLAN#	
31,97	PEG_CLKREQ2_LAN#	
60	CLK_REQ9_SATAE_N	
94	PEG_CLKREQ4_PCIE1#	
94	PEG_CLKREQ5_PCIE2#	
93	PEG_CLKREQ8_PCIE16#	

		XDP_CLK_CON#	XDP_CLK_CON
4	CPU1_PCBICLK_PCH#		
4	CPU1_PCBICLK_PCH		
63	PEG_CLK0_M2#		
63	PEG_CLK0_M2		
61	PEG_CLK1_WLAN#		
61	PEG_CLK1_WLAN		
31,97	PEG_CLK2_LAN#		
31,97	PEG_CLK2_LAN		
59	PEG_CLK3_PCH#		
59	PEG_CLK3_PCH		
94	PEG_CLK4_PCH#		
94	PEG_CLK4_PCH		
94	PEG_CLK5_PCH#		
94	PEG_CLK5_PCH		
93	PEG_CLK8_PCH#		
93	PEG_CLK8_PCH		

CLK OUT for CPU XDP

FOR PCIEx16 CONN

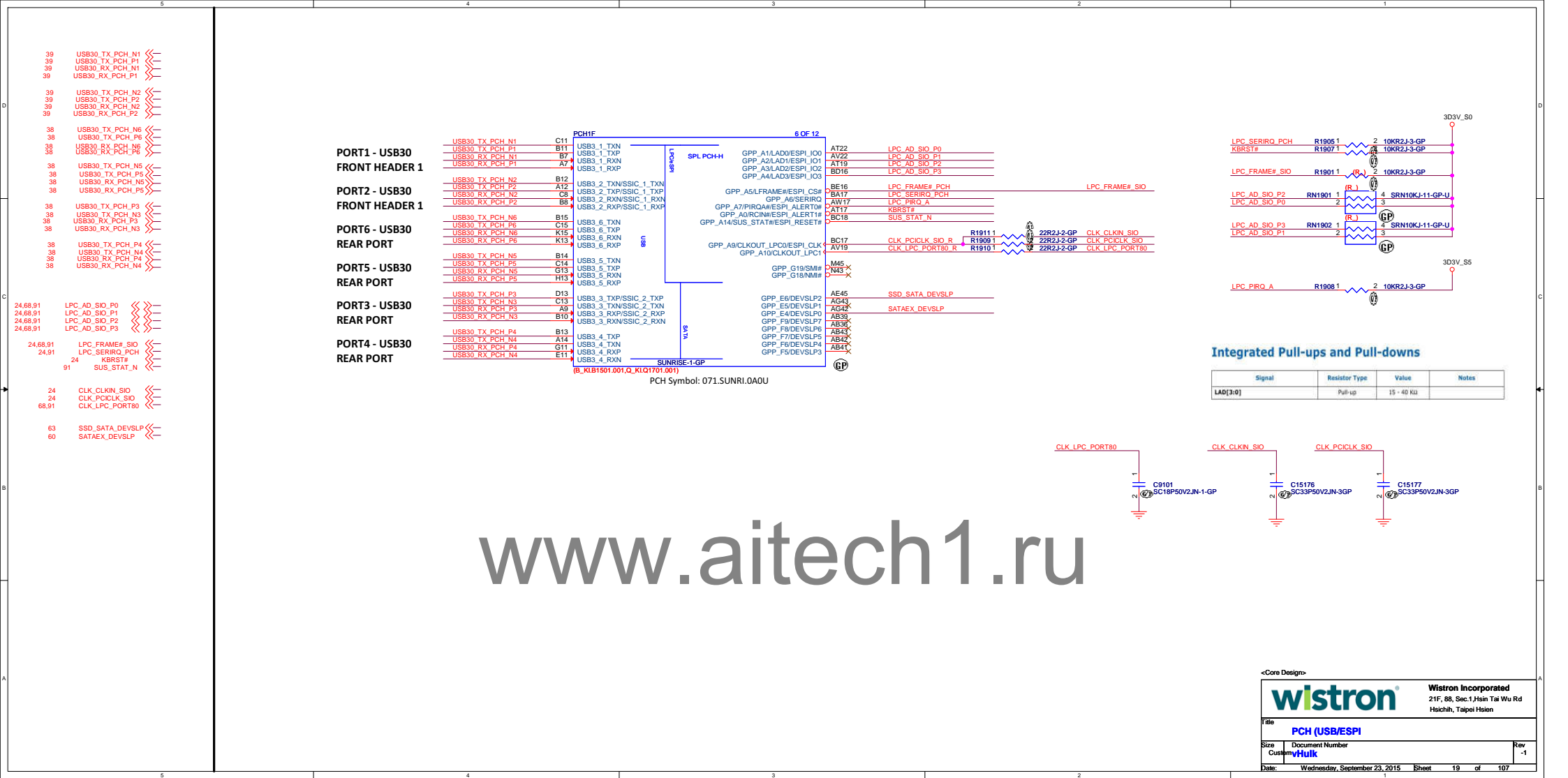
The image displays two circuit diagrams for the SCAP50V2CN-3GP, overlaid with a large watermark 'www.aitech1.ru'.

Left Diagram (Internal Oscillator Circuit):

- XTL_32K_X1_PCH** and **XTL_32K_X2_PCH** are connected to the oscillator circuit.
- X1801** is an **XTAL-320768KHZ-64-GP** crystal.
- X1802** is a **SC8P50V2CN-3GP** component.
- X1807** is a **1MR23-1-GP** component.
- C1801** is a **SC4P50V2CN-3GP** component with a value of **78.4R774.1FL**.
- C1804** is a **SC4P50V2CN-3GP** component with a value of **78.4R774.1FL**.
- C1803** is a **SC4P50V2CN-3GP** component with a value of **78.4R774.1FL**.
- The circuit is powered by **82.30001.661**.

Right Diagram (External Connections):

- XTL_24M_IN_PCH** and **XTL_24M_OUT_PCH** are connected to the oscillator circuit.
- X1802** is a **SC8P50V2CN-3GP** component.
- X1807** is a **1MR23-1-GP** component.
- C1803** is a **SC4P50V2CN-3GP** component with a value of **78.4R774.1FL**.
- C1804** is a **SC4P50V2CN-3GP** component with a value of **78.4R774.1FL**.
- C1801** is a **SC4P50V2CN-3GP** component with a value of **78.4R774.1FL**.
- C1802** is a **SC4P50V2CN-3GP** component with a value of **78.4R774.1FL**.
- C1803** is a **SC4P50V2CN-3GP** component with a value of **78.4R774.1FL**.
- C1804** is a **SC4P50V2CN-3GP** component with a value of **78.4R774.1FL**.



www.aitech1.ru

27	HDA_BITCLK_CODEC	⏏
27	HDA_RSTB_CODEC	⏏
27	HDA_SDIN0_PCH	⏏
27	HDA_SDOUT_CODEC	⏏
27	HDA_SYNC_CODEC	⏏
7	AUD_AZACPU_SDO_R	⏏
7	AUD_AZACPU_CPU_SDI	⏏
7	AUD_AZACPU_SCLK	⏏

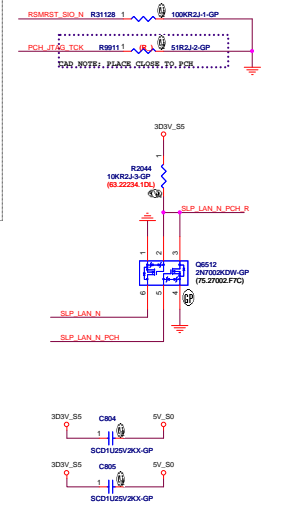
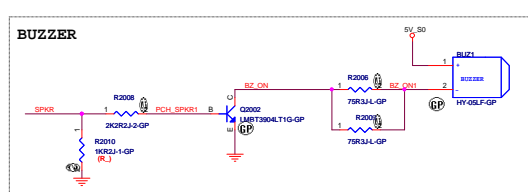
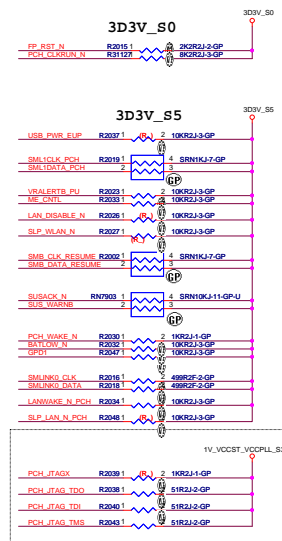
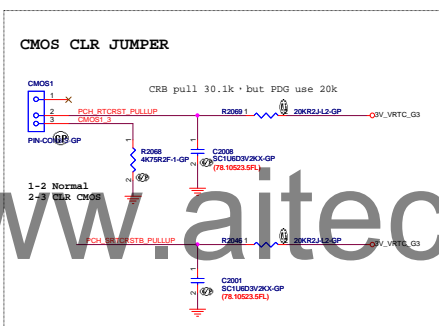
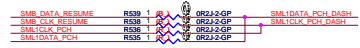
97	SMLINK0_CLK	三
97	SMLINK0_DATA	三
61	SMB_CLK_RESUME	三
61	SMB_DATA_RESUME	三
22	SMB_ALERT	三
31	SML1CLK_PCH_DASH	三
31	SML1DATA_PCH_DASH	三
59.93.94	SMB_CLK_MAIN	三
59.93.94	SMB_DATA_MAIN	三

40	PCH_FWPKW	➤➤
24	RSMRST_SIO_N	➤➤
11,12,13,14	SM_DRAMRST_K	➤➤
40	PCH_SYSPWKW	➤➤
24,40,41,42,43,44,50,8,24,42,44	SLP_S3_N	➤➤
	SLP_S4_N	➤➤
4	H_FWRGD	➤➤
24	PM_PVRSTN	➤➤
64	FP_RST_N	➤➤
59,61,63,93,94	PC_WAKE_N	➤➤
22	SUSCLK_PCH	➤➤

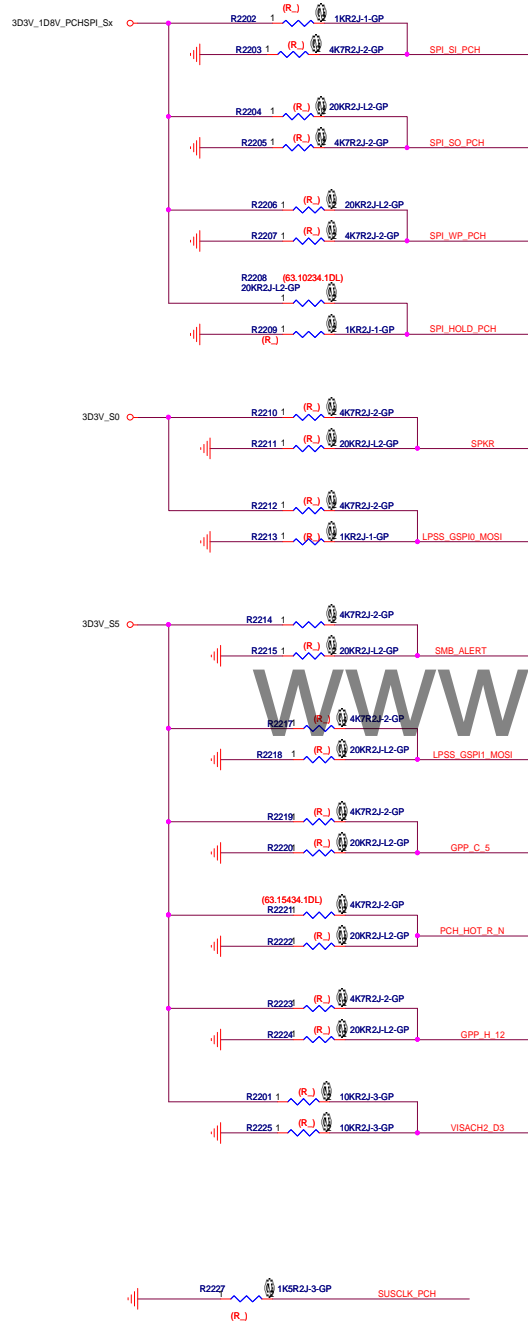
```

15      ME_CNTL >>
22      GPP_C_5 >>
22      PCH_HOT_R_N >>
22      SPIR <<
97      LAN_DISABLE_N <<
42      USB_PWR_EUP <<
24      SLP_LAN_N <<
24      LANWAKE_N_PCH <<
61      PCH_SUSCLK_WLAN <<
63      SUSCLK_PCH_M2 <<

```

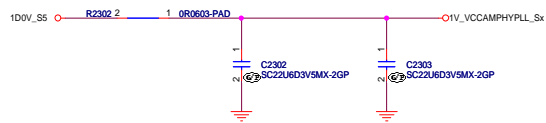


15,25 SPI_SI_PCH <<
15,25 SPI_SO_PCH <<
15,25,99 SPI_WP_PCH <<
15,25 SPI_HOLD_PCH <<
20 SPKR <<
15 LPSS_GSPI0_MOSI <<
20 SMB_ALERT <<
15 LPSS_GSPI1_MOSI <<
20 SUSCLK_PCH <<
20 GPP_C_5 <<
20 PCH_HOT_R_N <<
15 GPP_H_12 <<
16 VISACH2_D3 <<

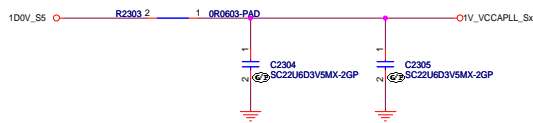


PCH STRAP FUNCTIONS

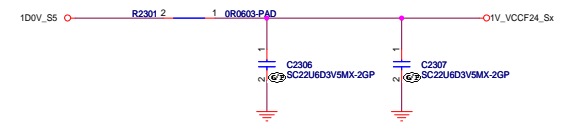
SPI_SI_PCH (SPI0_MOSI)	0: Enable boot halt 1: Disable boot halt The internal PU resistor is enabled when RSMRST# is asserted and is switched to the internal PD when RSMRST# is de-asserted.
SPI_SO_PCH (SPI0_MISO)	0: Disable JTAG ODT 1: Enable JTAG ODT The internal PU resistor is enabled when RSMRST# is asserted
SPI_WP_PCH (SPI0_IO2)	0: Enable consent strap 1: Disable consent strap PCH has internal weak PU
SPI_HOLD_PCH (SPI0_IO3)	0: Enable personality strap 1: Disable personality strap PCH has internal weak PU
SPKR (SPKR / GPP_B14)	0: Disable Top Swap mode. (Default) 1: Enable Top Swap mode. PCH internal pull-down is disabled after PLTRST# deasserts.
LPSS_GSPI0_MOSI (GPP_B18/GSPI0_MOSI)	0: Disable No Reboot mode. 1: Enable No Reboot mode This function is useful when running ITP/XDP. The internal pull-down is disabled after PLTRST# deasserts.
SMB_ALERT (GPP_C2/SMBALERT#)	0: Disable TSL confidentiality 1: Enable TSL confidentiality (default) The internal pull-down is disabled after RSMRST# deasserts.
LPSS_GSPI1_MOSI (GPP_B22/GSPI1_MOSI)	BOOT_SELECT STRAP 0: SPI select 1: LFC select The internal pull-down is disabled after PLTRST# deasserts.
GPP_C_5 (GPP_C5/SML0ALERT#)	ESPI/LPC SELECT STRAP 0: LPC is selected for EC. 1: eSPI is selected for EC. The internal pull-down is disabled after RSMRST# deasserts.
PCH_HOT_R_N (GPP_B23/SML1ALERT#/PCHHOT#)	0: Disable Exi boot stall bypass 1: Enable Exi boot stall bypass The internal PD resistor is disable after RSMRST# de-asserted.
GPP_H_12 (GPP_H12/SML2ALERT#)	ESPI flash sharing mode 0: Master attached flash sharing 1: Slave attached flash sharing PCH has internal weak PD.
VISACH2_D3 (GPP_E12)	DFX test mode 0: XTAL input is single ended. 1: XTAL input is differential. The internal PD resistor is disabled after RSMRST# de-asserts
HDA_SDOUT_PCH (HDA_SDO)	0: Enable security measures defined in the Flash Descriptor. 1: Disable Flash Descriptor Security (override). The internal pull-down is disabled after PLTRST# deasserts.
SUSCLK_PCH (GPD8/SUSCLK)	0: Disable OD PLL VR 1: Enable OD PLL VR



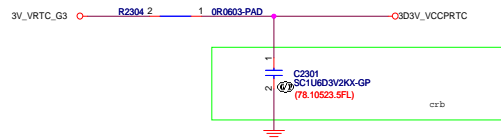
DESIGN NOTE:
PLACE HOLDER FOR VCCMPHYPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN A42,A43, AND B43



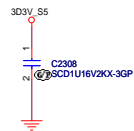
DESIGN NOTE:
PLACE HOLDER FOR VCCAPLL_1P0 AND VCCAAZPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN AJ5,AL5, AND AN19



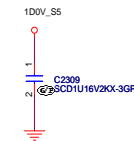
DESIGN NOTE:
PLACE HOLDER FOR VCCF24_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN K2 AND K3



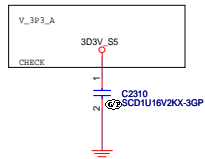
DESIGN NOTE:
BOARD CAP FOR VCCPRTC_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA22



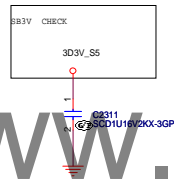
DESIGN NOTE:
EDGE CAP FOR VCCPGPPEF(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AJ41 AND AL41



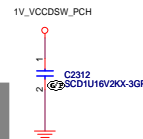
DESIGN NOTE:
BOAED CAP FOR VCCMPHY_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26



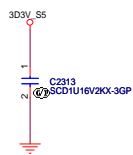
DESIGN NOTE:
EDGE CAP FOR VCCPUSBD5W_3P3
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN W15



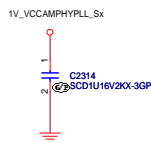
DESIGN NOTE:
BOAED CAP FOR VCCPRTCPRIM_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA20



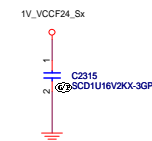
DESIGN NOTE:
BOAED CAP FOR VCCDSW_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA29



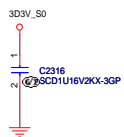
DESIGN NOTE:
EDGE CAP FOR VCCPGPPG(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AD41



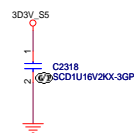
DESIGN NOTE:
BOAED CAP FOR VCCMPHYPLL_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN A42,A43 AND B43



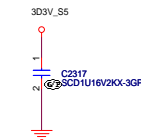
DESIGN NOTE:
BOAED CAP FOR VCCF24_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN K2,K3



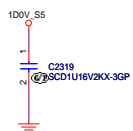
DESIGN NOTE:
BOAED CAP FOR VCCATS
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN AD13



DESIGN NOTE:
EDGE CAP FOR VCCPGPPBCH(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN BC42 AND BD40



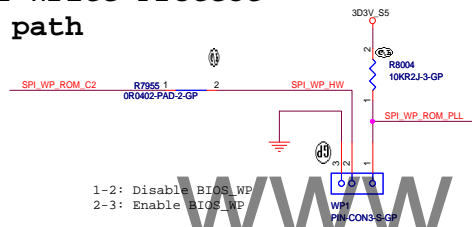
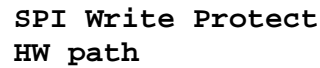
DESIGN NOTE:
BOAED CAP FOR VCCPHVC_3P3(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AN15



DESIGN NOTE:
EDGE CAP FOR VCCMPHY_1P0 AND VCCDUSB_1P0
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26, AND AC17

www.aitech1.ru

15	SPI_CS_PCH_N0	»»
15.22	SPI_SO_PCH	<<»»
15.22.99	SPI_WP_PCH	<<»»
15.22	SPI_HOLD_PCH<<»»	
15	SPI_CLK_PCH	»»
15.22	SPI_SI_PCH	<<»»
15	SPI_WP_ROM_C	»»
15	SPI_WP_ROM_C2	<<»»

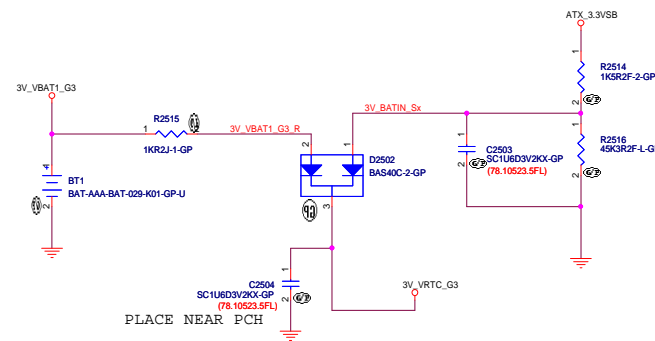


	Vendor	Package	SA	SB
Q170/B150	MXIC	SOP8 / 16MB	72.12873.001	72.12873.001
	WINBOND	SOP8 / 16MB	72.25128.0E1	72.25128.0E1

Disable BIOS_WP
Enable BIOS_WP

WP1
PIN-CON3-S-GP

www.aitech1.ru



An Intel internal debug strap is implemented on the SPI0_IO3 signal. However, the strap is not functioning as expected on ES (SKL U/Y platform) and pre-E51/E51 (SKL S/H platform) samples and could prevent the system from booting. The issue will be fixed in future samples.

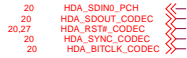
To ensure the platform boots with these early samples, Intel recommends customers to implement a pull-down resistor on the SPI0_IO3 signal aside from the 1 kOhm pull-up resistor which is already a requirement on the signal. There are two options to implement the pull-down resistor:

Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

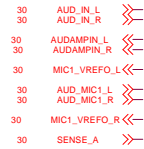
Option 2: Implement a strong pull-down resistor (e.g. 100 Ohm) on the signal and disable it after RSMRST# de-assertion.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

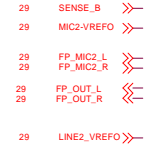
HD_LINK



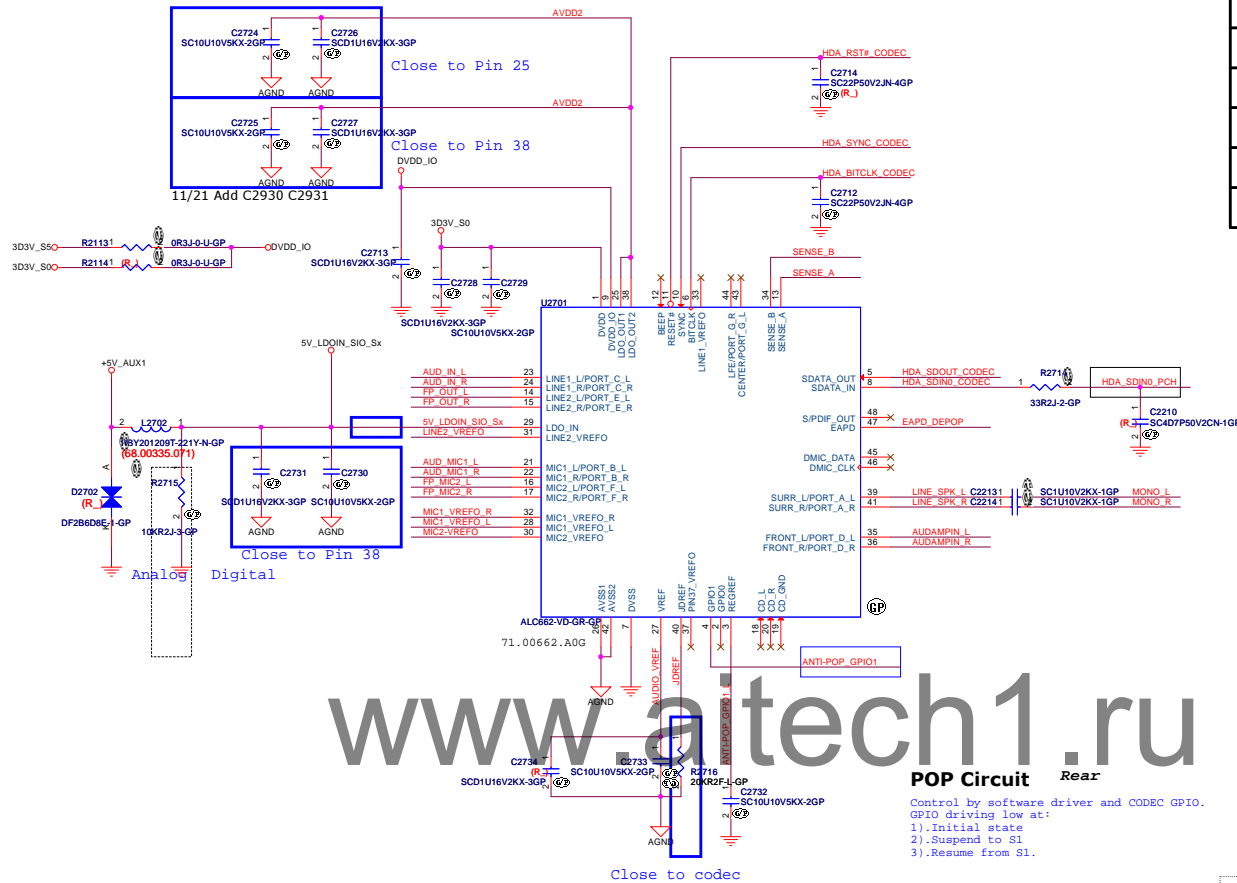
AUDIO REAR PORT



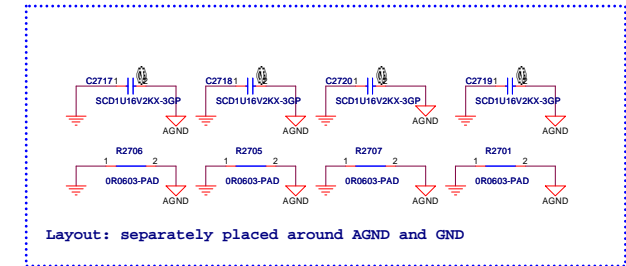
AUDIO FRONT HEADER



MISC



	ALC662-VC\VD
Line-in	pin23/24
Line-out	pin35/36
Mic-in 1	pin21/22
Mic-in 2	pin16/17
FP-out	pin14/15

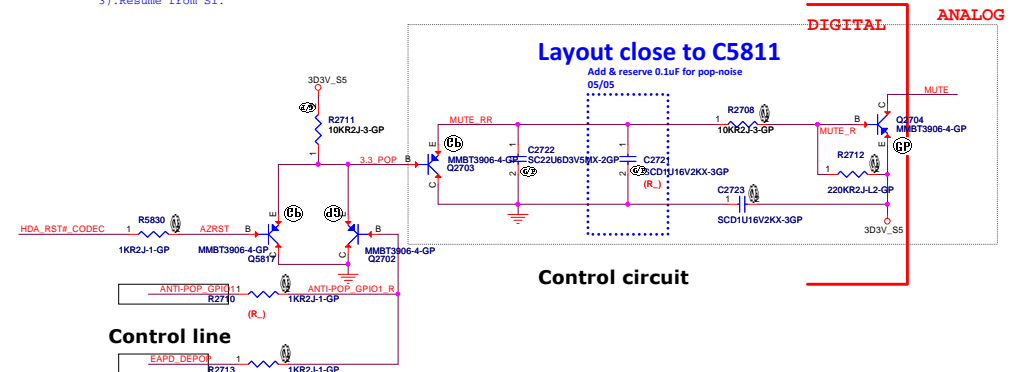
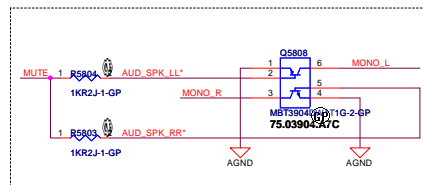
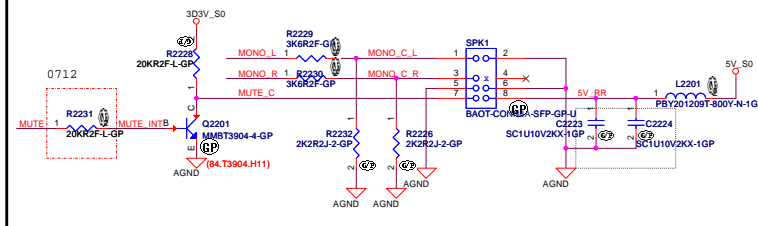


www.aitech1.ru

POP Circuit Rear


Control by software driver and CODEC GPIO.
GPIO driving low at:
1).Initial state
2).Suspend to S1
3).Resume from S1.

Audio Internal Speaker Header



<Core Design>

(R)
www.aitech1.ru

<Core Design>	
 Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Haichih, Taipei Hsien	
Title	
AMP_(R)	
Size	Document Number
C	vHulk
Date:	Wednesday, September 23, 2015
Sheet	28 of 107
Rev	-1

15 FP_AUDIO_PRESENCE_N <<--

27 SENSE_B <<--

27 MIC2_VREF0 <<--

27 FP_MIC2_L <<--

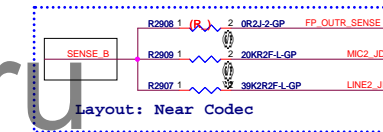
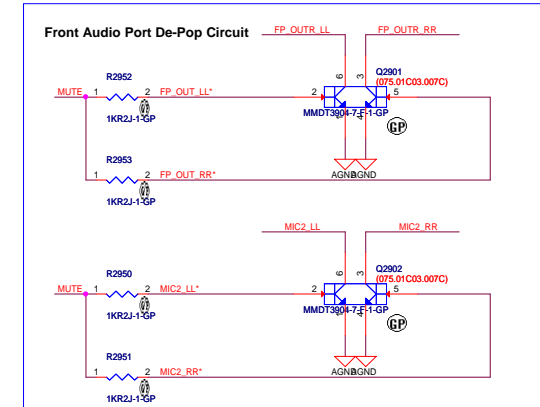
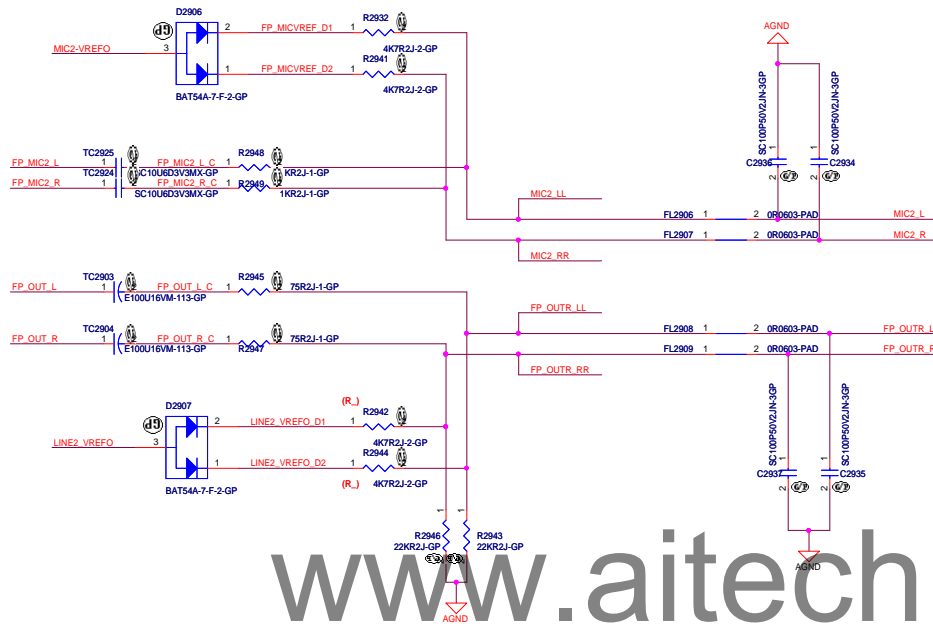
27 FP_MIC2_R <<--

27 FP_OUT_L <<--

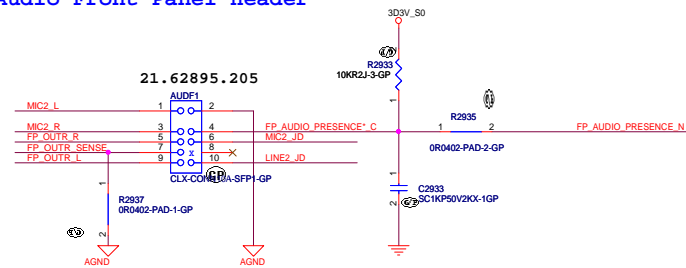
27 FP_OUT_R <<--

27 LINE2_VREF0 <<--

27,30 MUTE >>--



Audio Front Panel Header



AUDIO REAR PORT

27 AUD_IN_L <<<
27 AUD_IN_R <<<
27 AUDAMPIN_L >>>
27 AUDAMPIN_R >>>
27 MIC1_VREF0_L >>>
27 AUD_MIC1_L >>>
27 AUD_MIC1_R >>>
27 MIC1_VREF0_R >>>

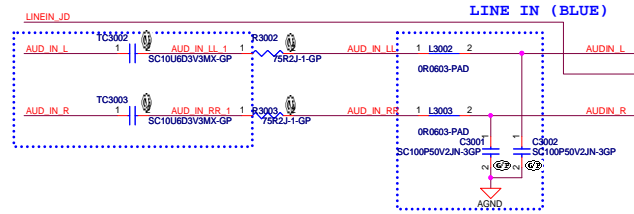
27 SENSE_A <<<
27,29 MUTE >>>

The cap need to close codec on layout.

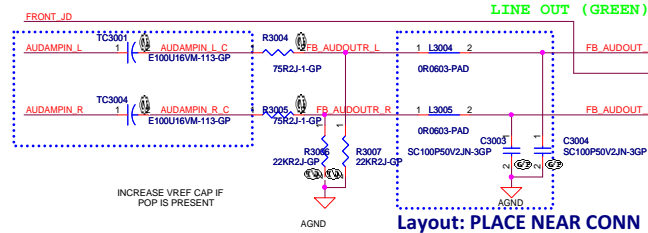
The cap need to close codec on layout.

The cap need to close codec on layout.

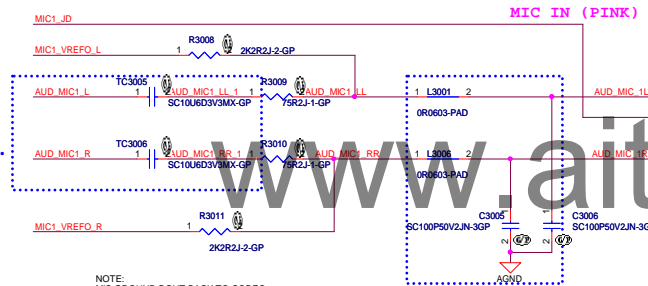
BACK PANEL PHONJACKS



Layout: PLACE NEAR CONN

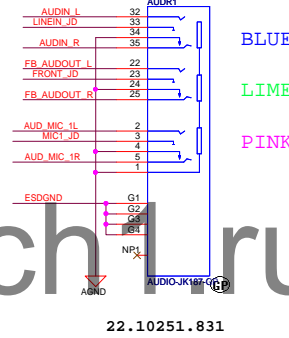


Layout: PLACE NEAR CONN

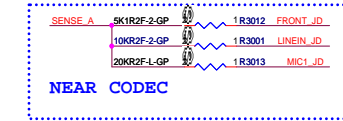
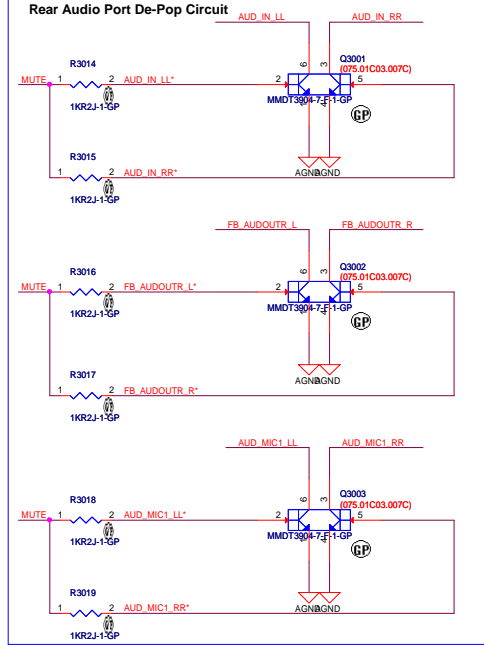


Layout: PLACE NEAR CONN

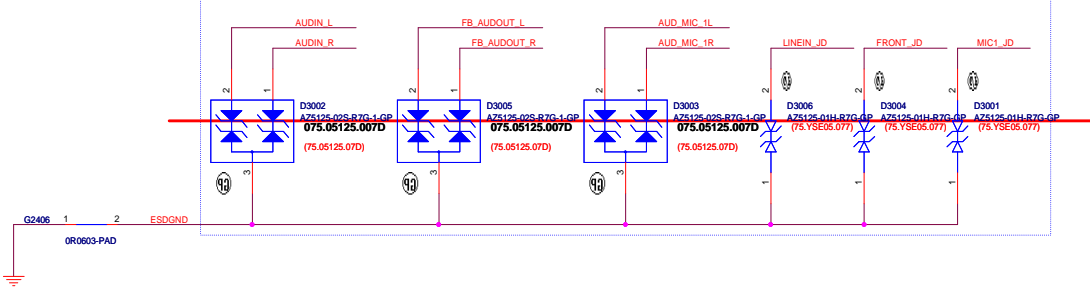
NOTE:
MIC GROUND ROUT BACK TO CODEC
ALONG WITH MIC TRACE.
TIE MIC_GND TO AGND NEAR CODEC



22.10251.831



audio ESD design



MDI

32.97	LAN_MDI_LAN_P0	»»»
32.97	LAN_MDI_LAN_N0	
32.97	LAN_MDI_LAN_P1	»»»
32.97	LAN_MDI_LAN_N1	
32.97	LAN_MDI_LAN_P2	»»»
32.97	LAN_MDI_LAN_N2	
32.97	LAN_MDI_LAN_P3	»»»
32.97	LAN_MDI_LAN_N3	

PCIE

16,97	PEG_CLK2_LAN	→
16,97	PEG_CLK2_LAN#	→
16,97	PCIE_TX_LAN_P5	←
16,97	PCIE_TX_LAN_N5	←
16,97	PCIE_RX_LAN_P5	←
16,97	PCIE_RX_LAN_N5	←

OTHERS

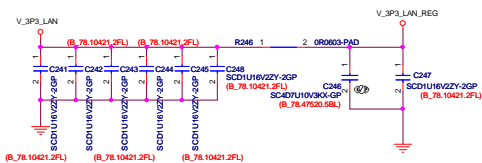
24	PLTRST_LAN	>>
24,97	LANWAKE_N	<<
,97	PEG_CLKREQ2_LAN#	<<

LAN LED

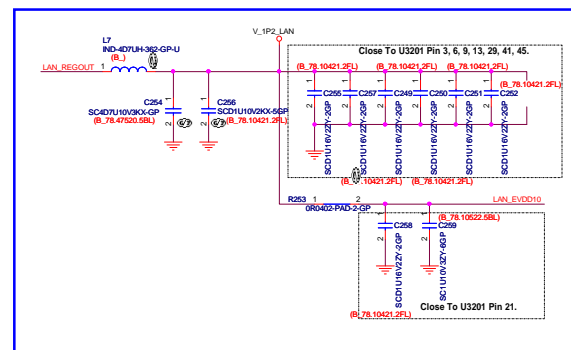
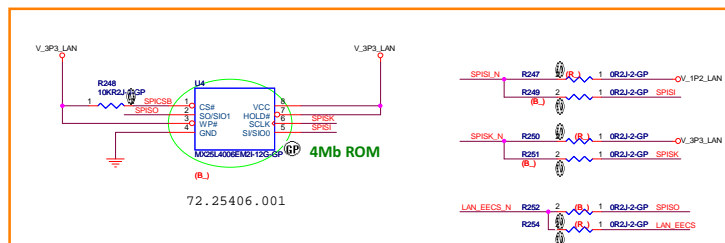
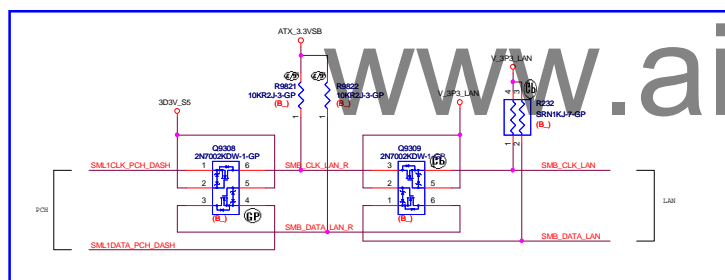
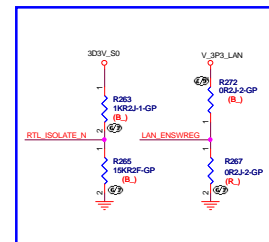
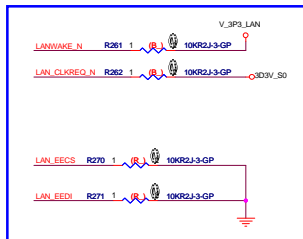
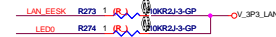
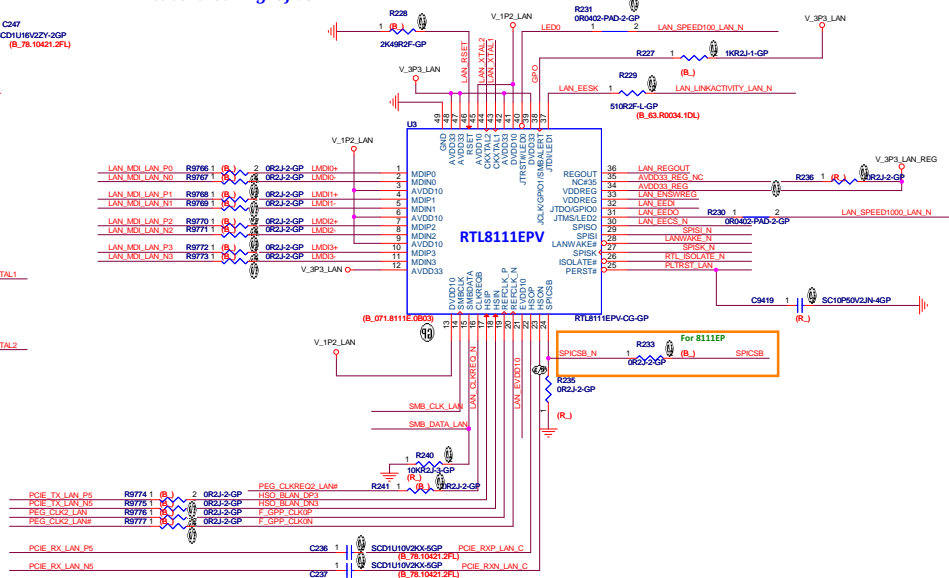
32,97	LAN_SPEED1000_LAN_N	»»
32,97	LAN_SPEED100_LAN_N	»»
32,64,97	LAN_LINKACTIVITY_LAN_N	»»

SMBUS

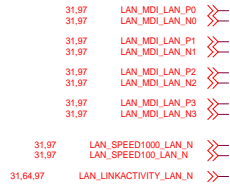
20	SML1CLK_PCH_DASH	<<>>
20	SML1DATA_PCH_DASH	<<>>
24	SMB_CLK_LANE	<<>>
24	SMB_DATA_LANE	<<>>



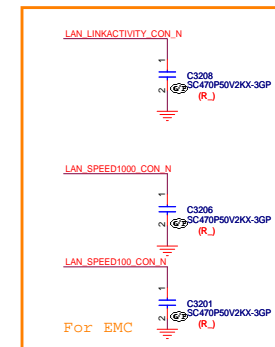
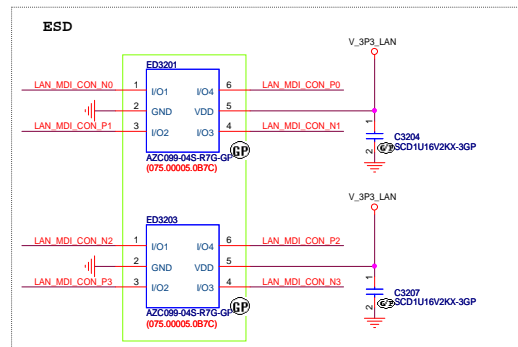
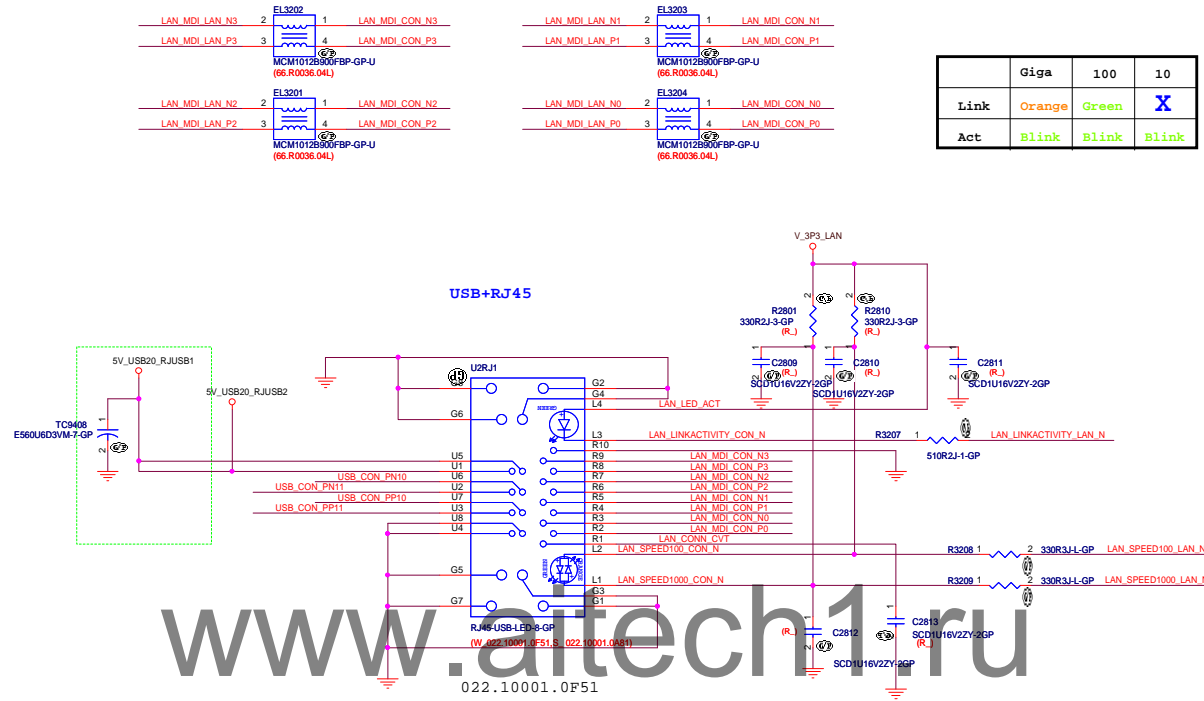
10Mb: Green
100Mb: Green
1Gb: Orange
Active: Green Light flash




LAN



LAN



(R)
www.aitech1.ru

<Core Design>	
 Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Haichih, Taipei Hsien	
Title Card Reader (R)	
Size C	Document Number vHulk
Date: Wednesday, September 23, 2015	Rev -1
Sheet 33 of 107	

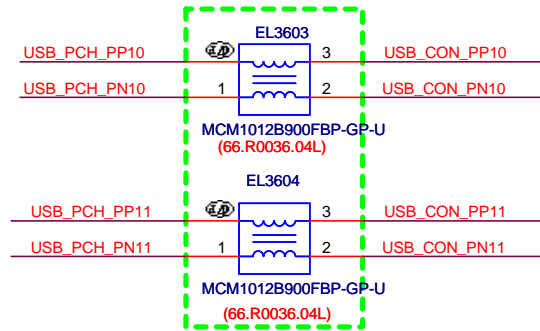
(R)
www.aitech1.ru

(R)
www.aitech1.ru

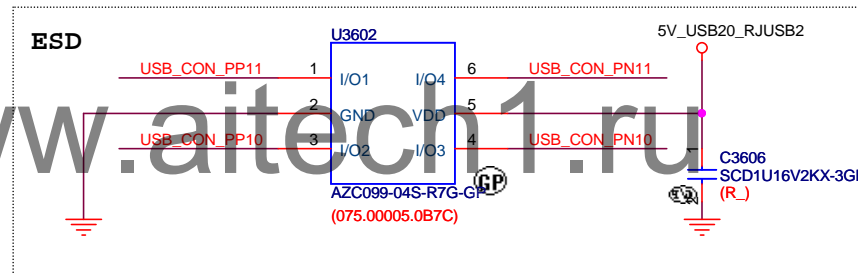
USB 2.0 Rear Signals for RJ45/USB2.0 Stack

16	USB_PCH_PP10	⏏
16	USB_PCH_PN10	⏏
16	USB_PCH_PP11	⏏
16	USB_PCH_PN11	⏏
32	USB_CON_PP10	⏏
32	USB_CON_PN10	⏏
32	USB_CON_PP11	⏏
32	USB_CON_PN11	⏏

USB 2.0 Rear Signals for RJ45/USB2.0 Stack



DESIGN NOTE:
To U2RJ1(U2+RJ45 CONN)
IF SI Concern, Change CMC PN:068.01012.2001



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title
USB 20_REAR PORT

Size
Custom **vHulk**

Rev
-1

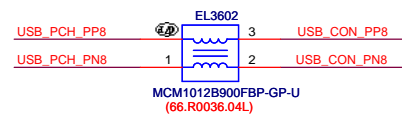
Date: Wednesday, September 23, 2015 Sheet 36 of 107

CR HEADER

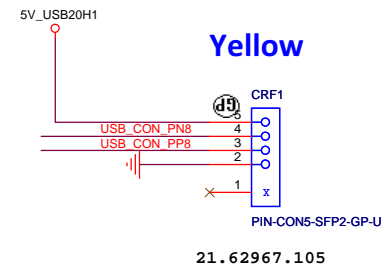
16 USB_PCH_PP8
16 USB_PCH_PN8

16 USB_PCH_PP9
16 USB_PCH_PN9

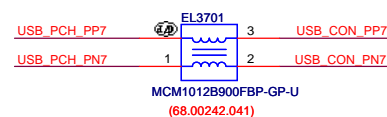
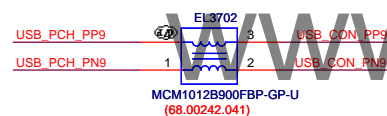
16 USB_PCH_PP7
16 USB_PCH_PN7



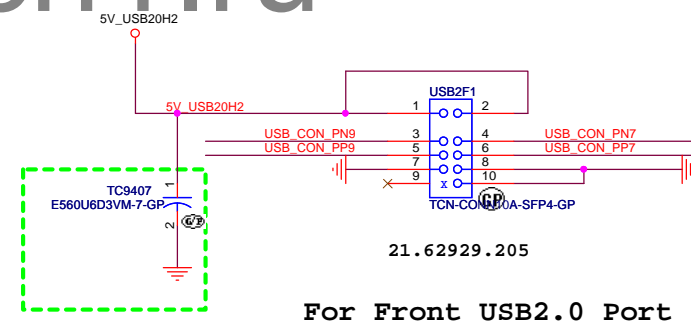
ESD



USB2.0 FRONT HEADER



ESD



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

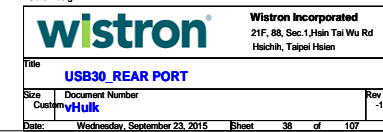
Title
USB20_FRONT HEADER

Size Document Number
Custom **vHulk**

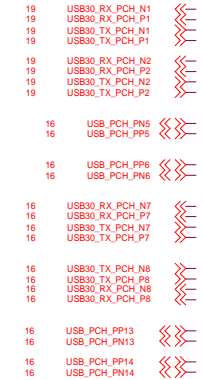
Rev
-1

Date: Wednesday, September 23, 2015 Sheet 37 of 107

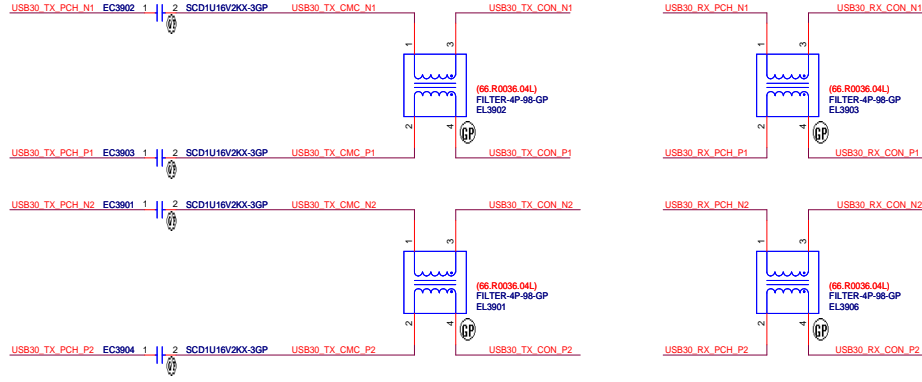
<Core Design>



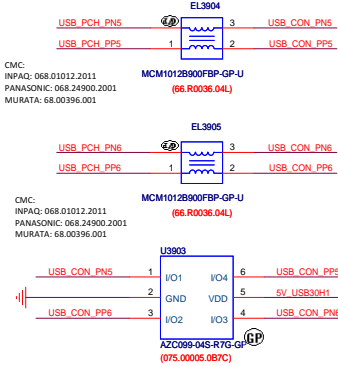
USB3.0 FRONT HEADER



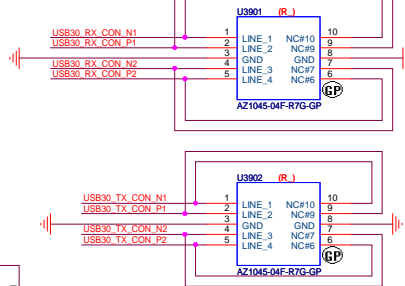
USB3.0 EMI



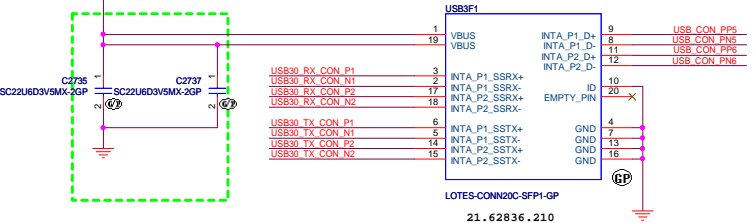
EMI



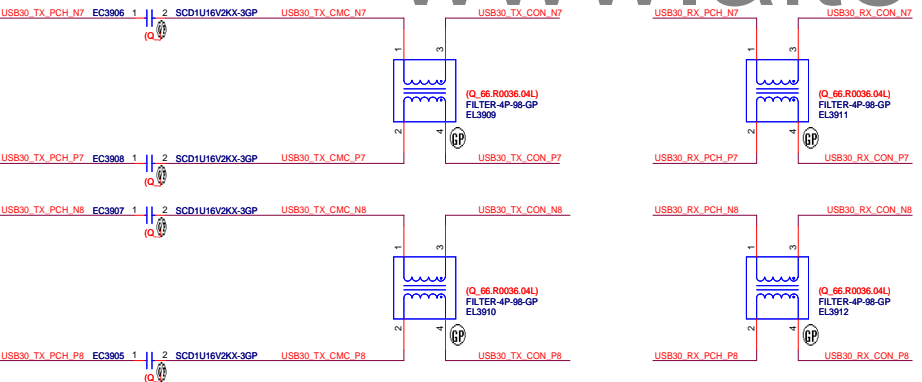
ESD



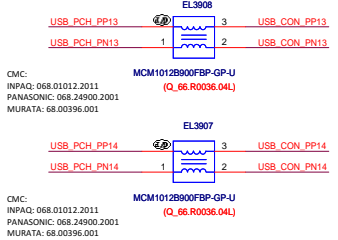
USB3.0 FRONT HEADER 1



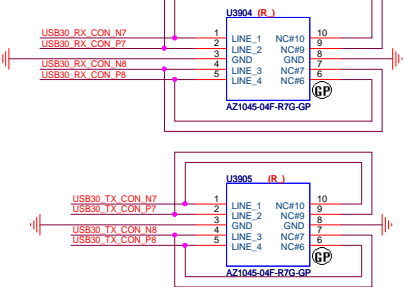
USB3.0 EMI



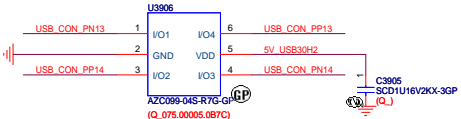
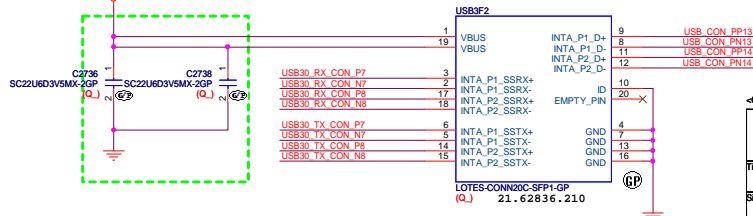
EMI



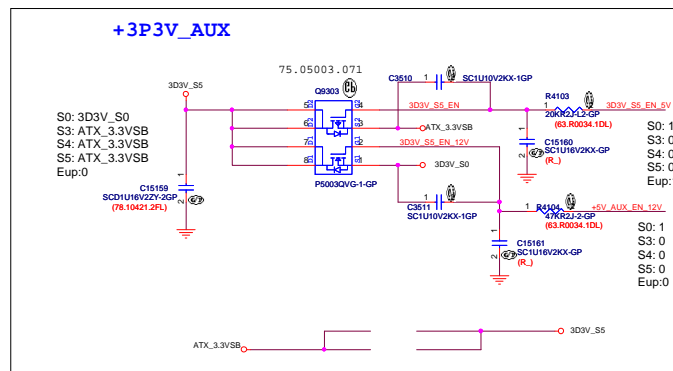
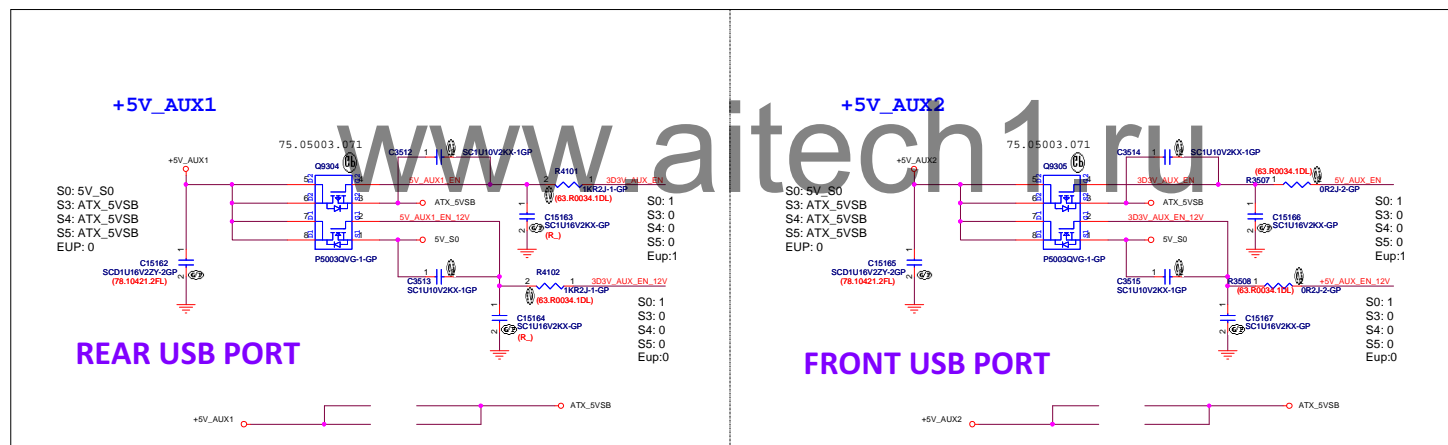
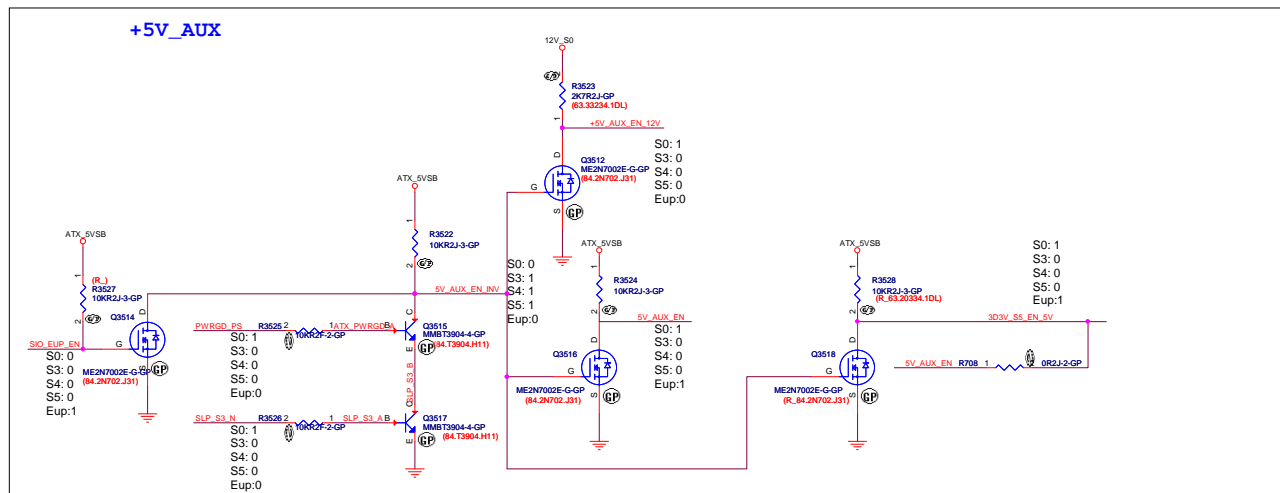
ESD



USB3.0 FRONT HEADER2(Q170 SKU)

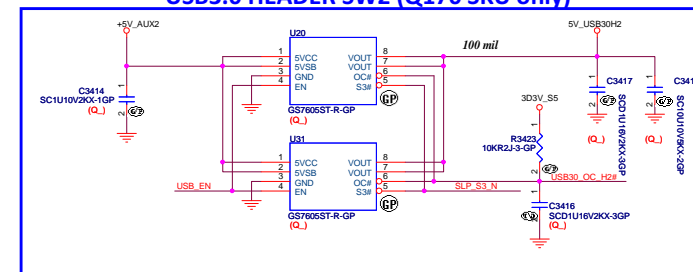


Dual Power Control GROUP A POWER(S5_EuP)



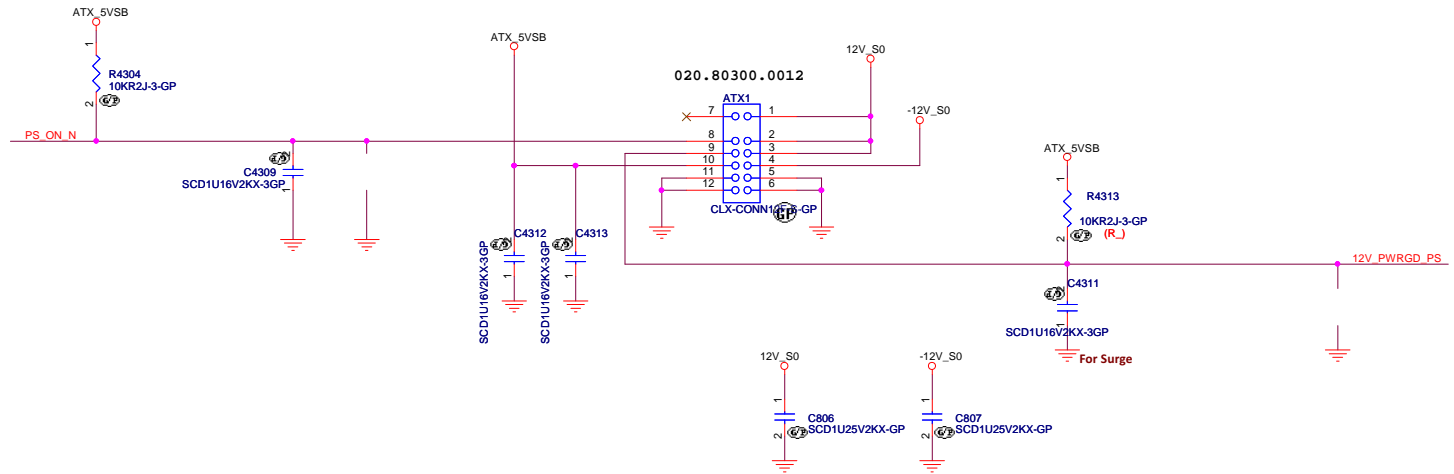
	SIO_EUP_EN	SLP_S3_N	+5V_AUX1	+5V_AUX2
S0	0	1	5V_S0	5V_S0
S3	0	0	ATX_5VSB	ATX_5VSB
S4	0	0	ATX_5VSB	ATX_5VSB
S5	0 (EUP Disable)	0	ATX_5VSB	ATX_5VSB
S5	1 (EUP Enable)	0	No Power	No Power

S4, S5 --> choice by USB_PWR_SLP
S3-S0 --> choice by SLP_S4#

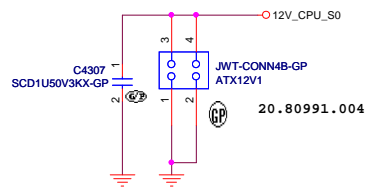


24 PS_ON_N >>
20,24,40,41,42,44,50 SLP_S3_N >>
49 12V_PWRGD_PS <<

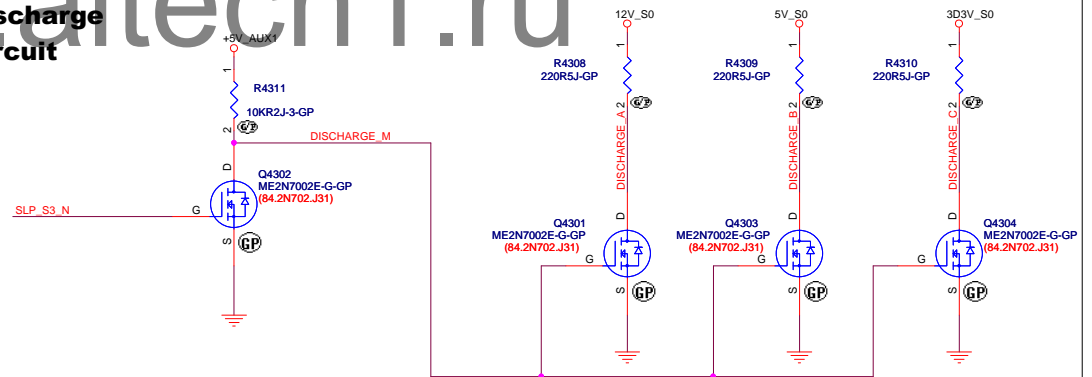
ATX CONNECTOR



CPU PWR CONN



Discharge Circuit



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

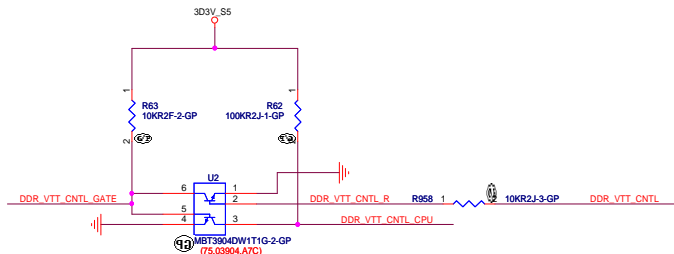
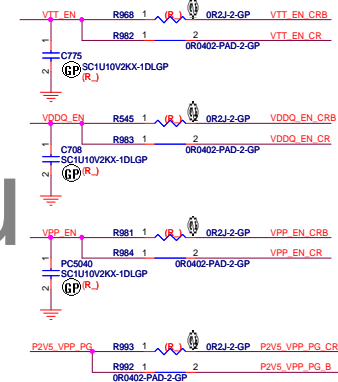
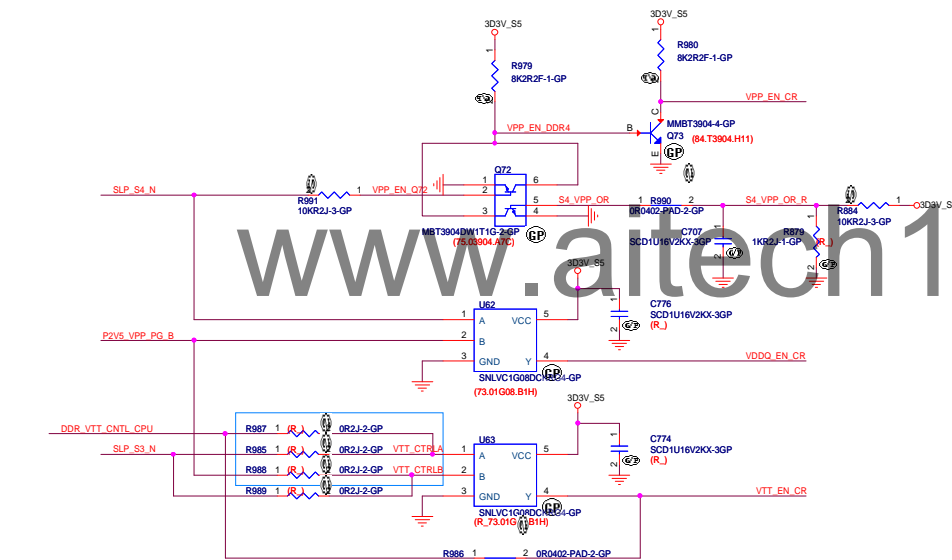
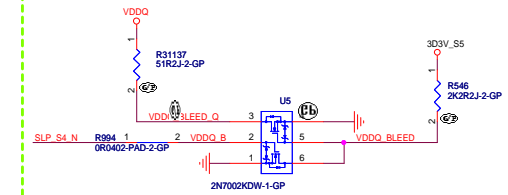
Title

ATX

Size Document Number
Customer **HyHulk**

Rev
-1

Date: Wednesday, September 23, 2015 Sheet 43 of 107



VCC5A/VCC3A

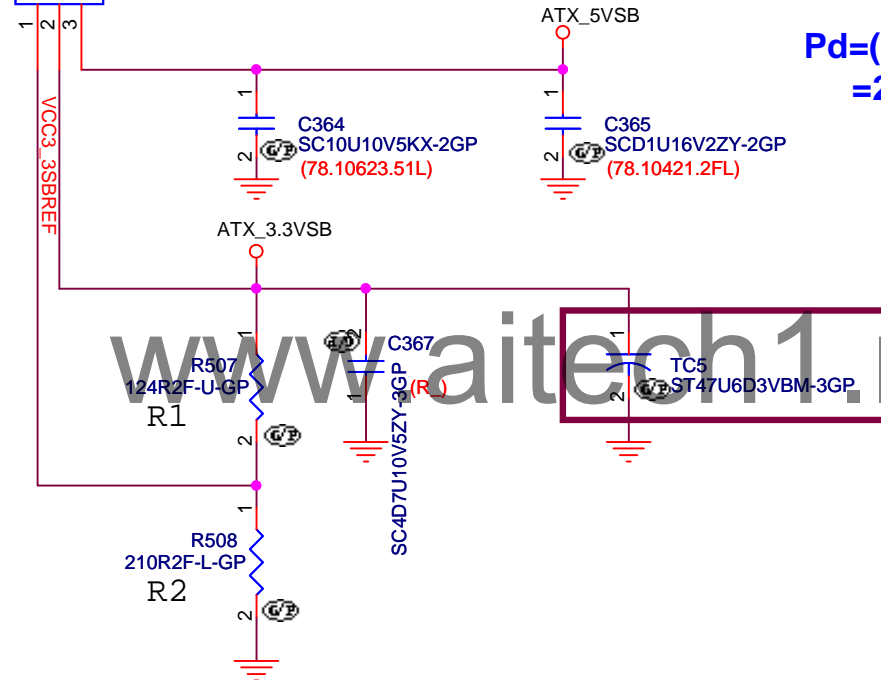
V_3P3_A 1.5A

U16
APL1085UC-GP
(074.01085.0A3M)

$$1.25/(R1/(R1+R2))=3.36V$$

S3/S4/S5 : Low Only . (Standby Power)
S0 : High_11.7V (Normal Power)

$$P_d=(5-3.3)*1.5=2.55W$$



<Core Design>

wistron

Wistron Incorporated

21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title

DCDC-3D3V&5V

Size

A

Document Number

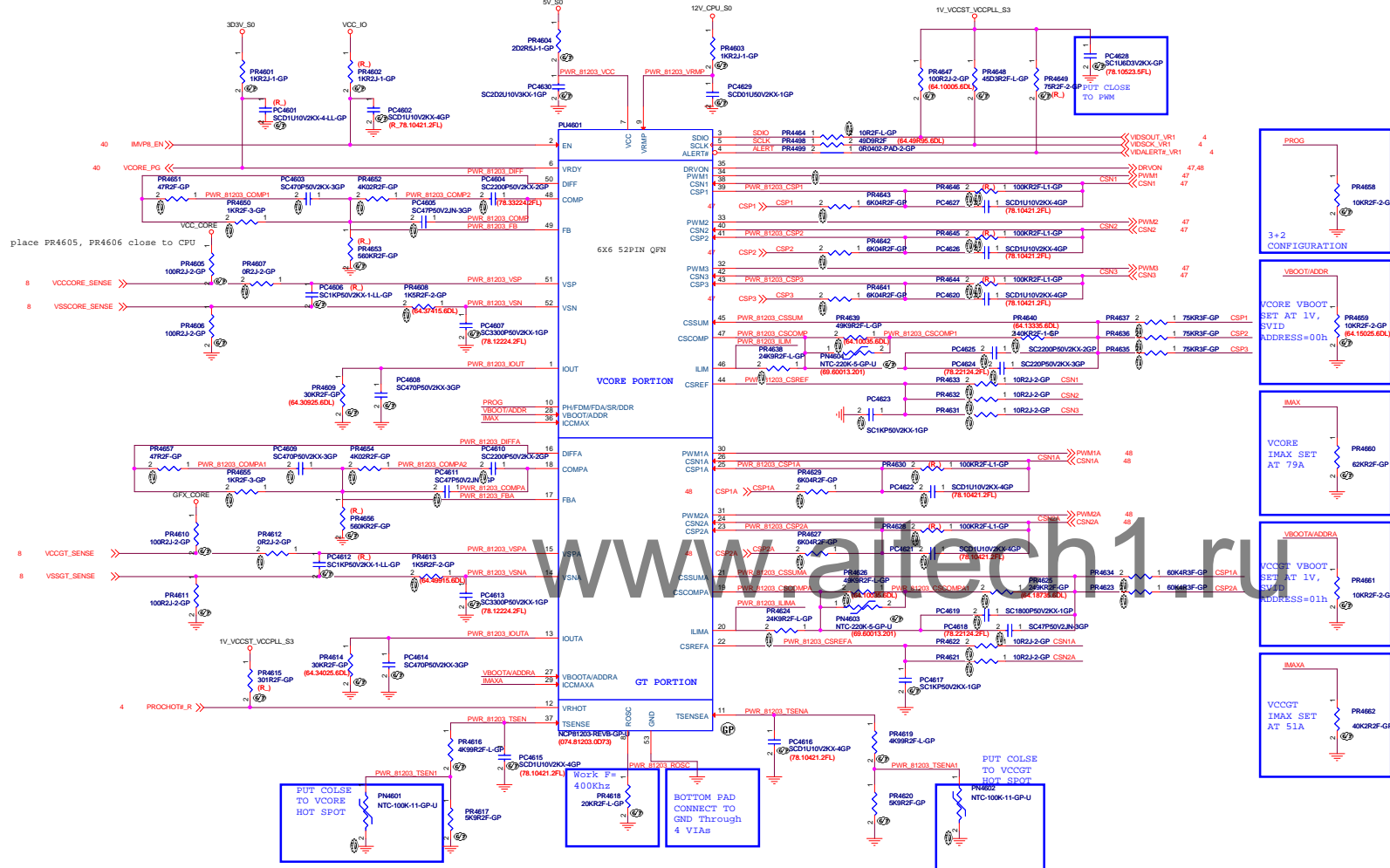
vHulk

Rev

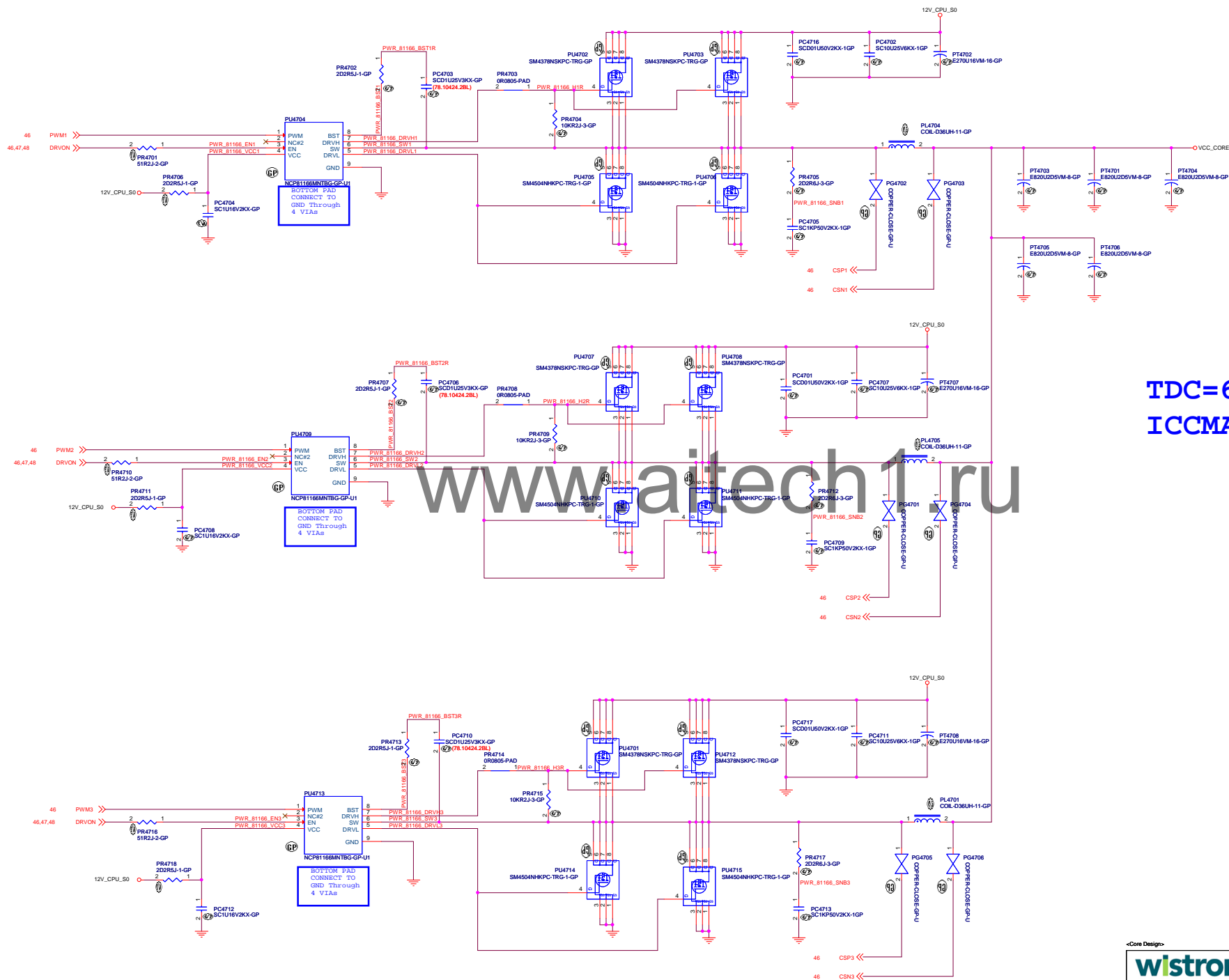
-1

Date: Wednesday, September 23, 2015 Sheet 45 of 107

Intel SKYLAKE IMVP8 POWER CKT -
3+2 PHASE



Vin ripple=10.48A



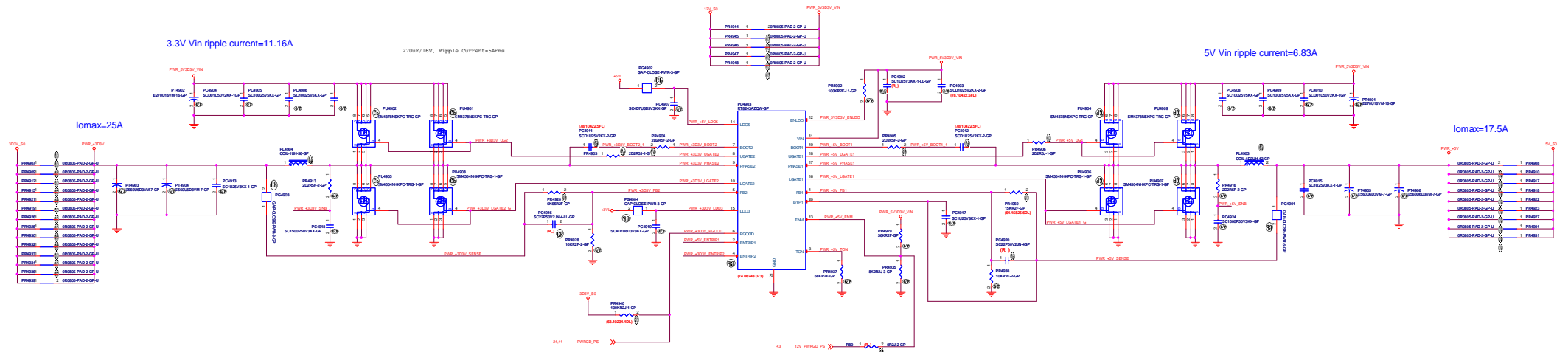
TDC=64A
ICCMAX=86A

PWR_3D3V/PWR_5V

3.3V Vin ripple current=11.16A

270uF/16V, Ripple Current=5Amm

5V Vin ripple current=6.83A



www.aitech1.ru

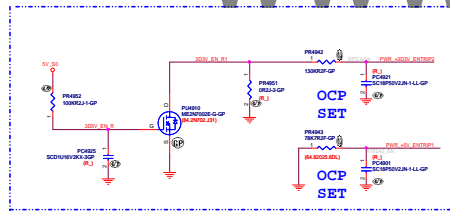


Table 2. Power Up Sequencing(RT8243A)

ENLDO(V)	ENLDO	ENTRIP1	ENTRIP2	LDO5(V)	LDO3(V)	SWP1	SWP2
LOW	LOW	X	X	OEE	OEE	OEE	OEE
>1.5V	LOW	X	X	On	On	OEE	OEE
>1.5V	>1.5V	OEE	OEE	On	On	OEE	OEE
>1.5V	>1.5V	OEE	On	On	On	OEE	On
>1.5V	>1.5V	On	On	On	On	On	On
>1.5V	>1.5V	On	OEE	On	On	On	On

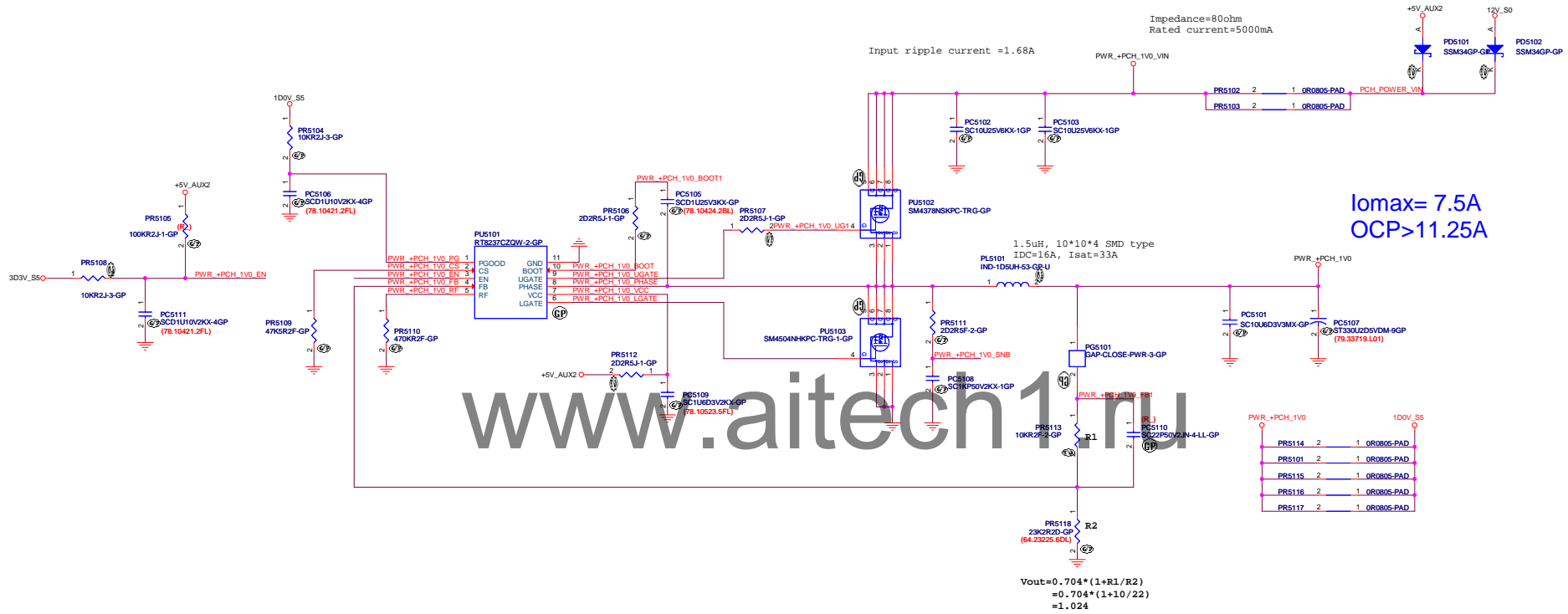
Vin ripple current=1.68A

Input ripple current = 1.68A

Impedance=80ohm
Rated current=5000mA

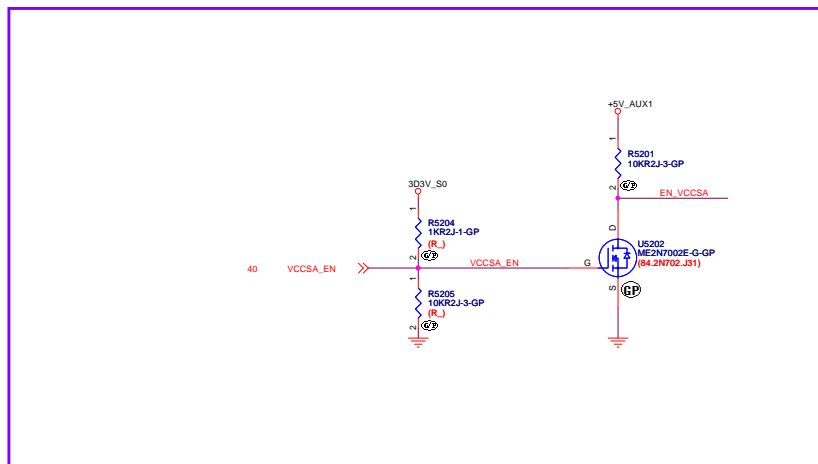
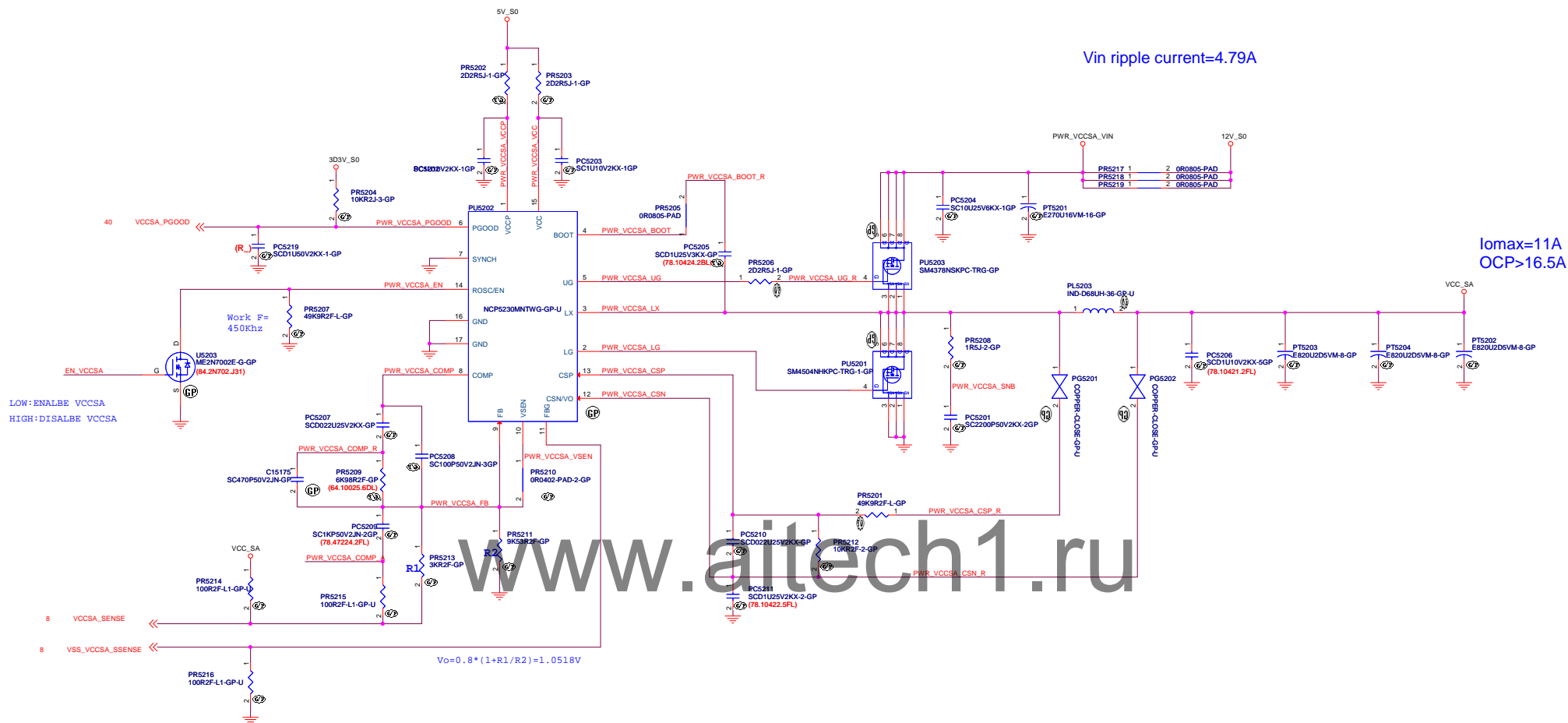
I_{omax} = 7.5A
OCP > 11.25A

$$V_{out} = 0.704 * (1 + R1/R2) \\ = 0.704 * (1 + 10/22) \\ = 1.024$$



<Core Design>

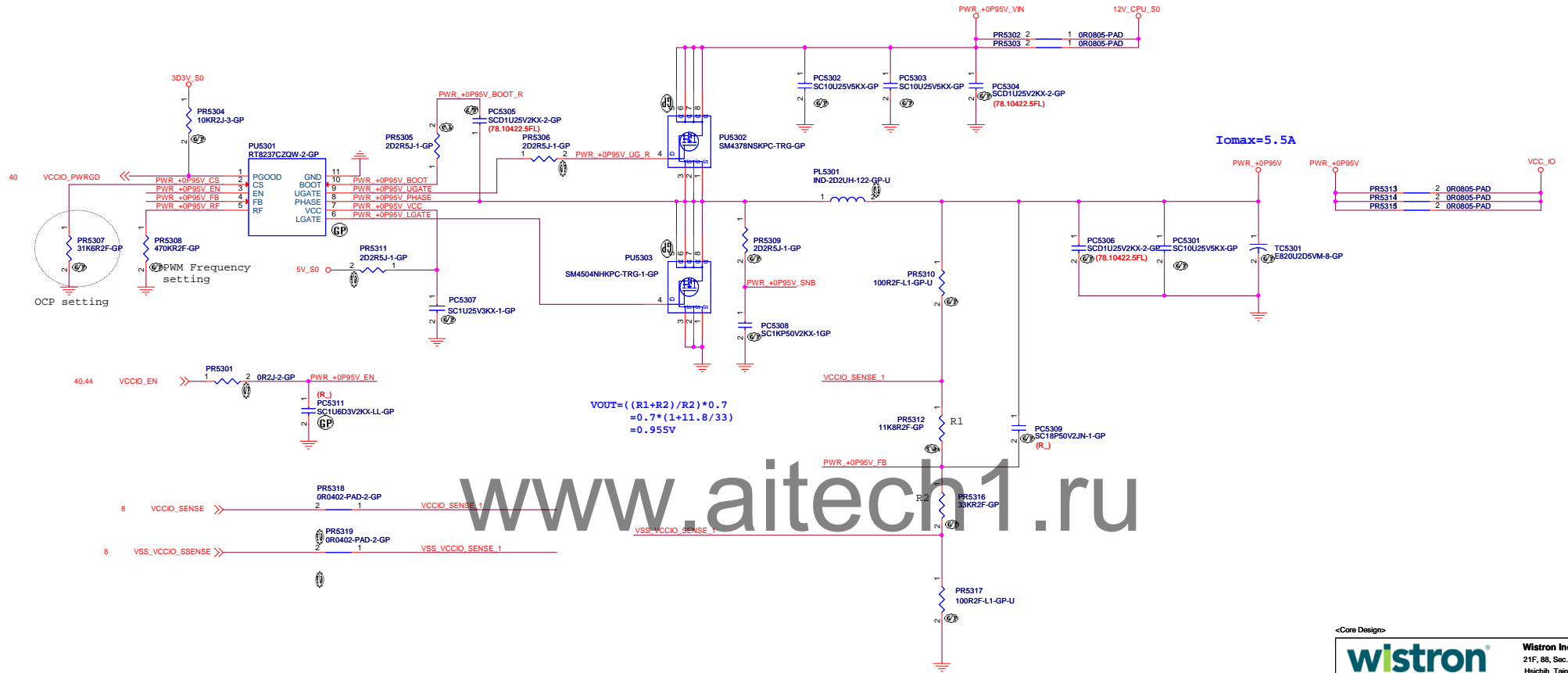
wistron		Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title		PCH_1P0V (RT8237C)	
Size	Document Number	Rev	
Customer	Hulk	1	
Date	Wednesday, September 23, 2015	Sheet	51 of 107



<Core Design>

wistron		Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsinchi, Taipei Hsien	
File VCC_SA(NCP5230M)			
Size	Document Number		Rev
Customer	Hulk		-1
Date:	Wednesday, September 23, 2015	Sheet	52 of 107

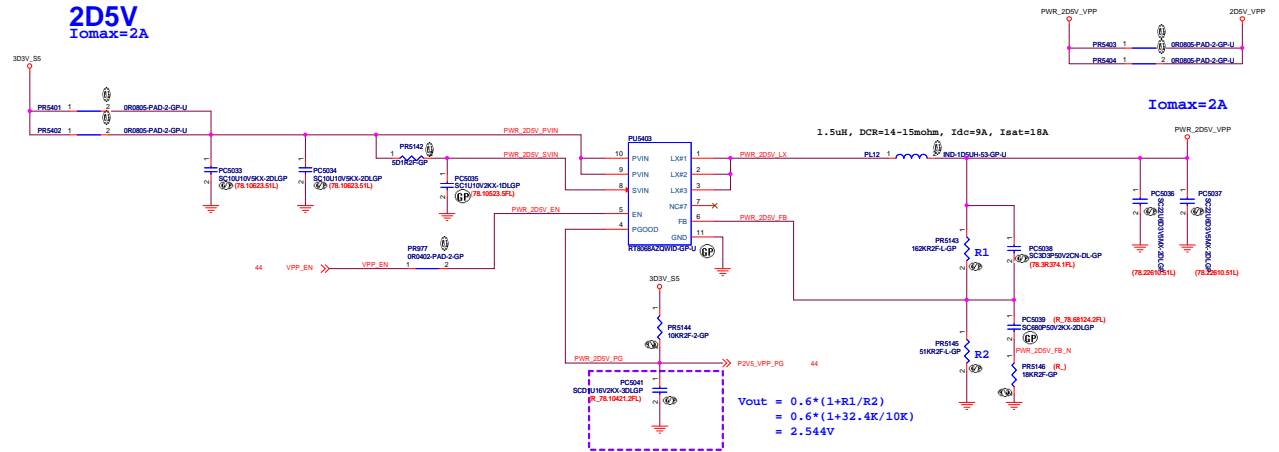
VCCIO



www.aitech1.ru

<Core Design>

wistron		Wistron Incorporated	
		21F, 88, Sec.1 Hsin Tai Wu Rd	
		Hsichih, Taipei Hsien	
Title			
VCC_IO(RT8237C)			
Size	Document Number		Rev
Customer	vHulk		-1
Date:	Wednesday, September 23, 2015		Sheet 53 of 107

$$\begin{aligned} V_{out} &= 0.6 \cdot (1 + R_1/R_2) \\ &= 0.6 \cdot (1 + 32.4\text{K}/10\text{K}) \\ &= 2.544\text{V} \end{aligned}$$


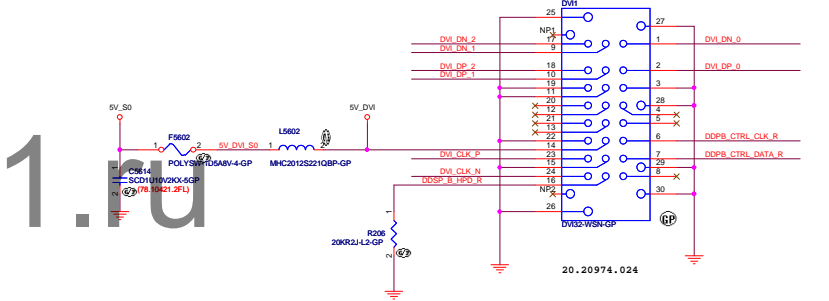
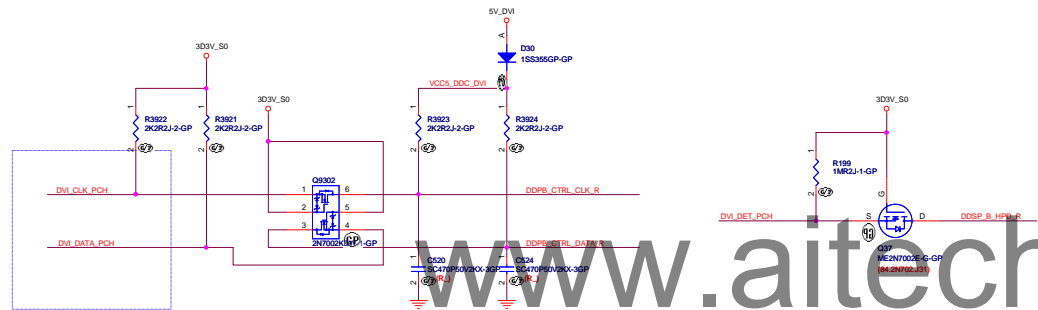
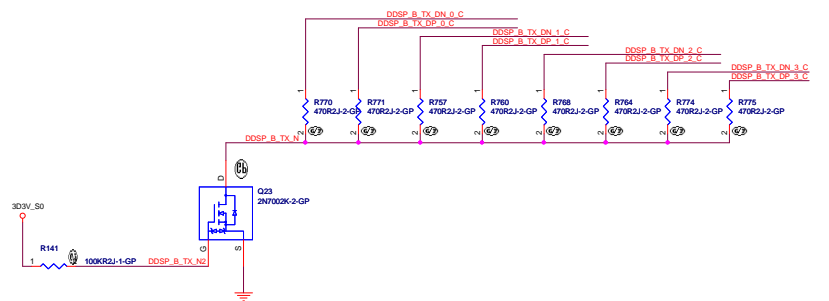
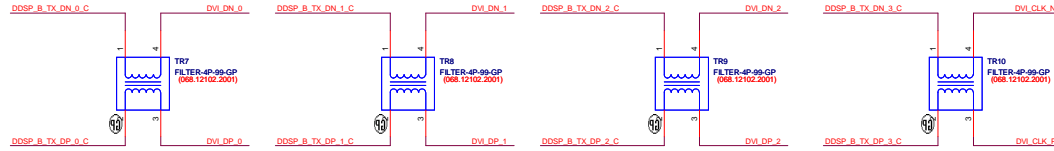
2014/8/26
Del 1D8V_S5

www.aitech1.ru

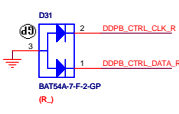
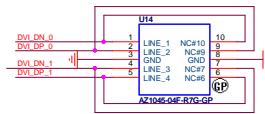
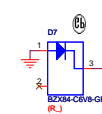
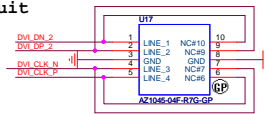
DDI PORT B

7 DVI_DATA_CPU_P0
7 DVI_DATA_CPU_N0
7 DVI_DATA_CPU_P1
7 DVI_DATA_CPU_N1
7 DVI_DATA_CPU_P2
7 DVI_DATA_CPU_N2
7 DVI_DATA_CPU_P3
7 DVI_DATA_CPU_N3
16 DVI_CLK_PCH
16 DVI_DET_PCH

DVI_DATA_CPU_P0	C80	1	2	SCD1U10V2KX-4GP	(78.10421.2FL)	DDSP_B_TX_DN_0.C
DVI_DATA_CPU_N0	C82	1	2	SCD1U10V2KX-4GP	(78.10421.2FL)	DDSP_B_TX_DP_0.C
DVI_DATA_CPU_P1	C81	1	2	SCD1U10V2KX-4GP	(78.10421.2FL)	DDSP_B_TX_DN_1.C
DVI_DATA_CPU_N1	C85	1	2	SCD1U10V2KX-4GP	(78.10421.2FL)	DDSP_B_TX_DP_1.C
DVI_DATA_CPU_P2	C89	1	2	SCD1U10V2KX-4GP	(78.10421.2FL)	DDSP_B_TX_DN_2.C
DVI_DATA_CPU_N2	C87	1	2	SCD1U10V2KX-4GP	(78.10421.2FL)	DDSP_B_TX_DP_2.C
DVI_DATA_CPU_P3	C83	1	2	SCD1U10V2KX-4GP	(78.10421.2FL)	DDSP_B_TX_DN_3.C
DVI_DATA_CPU_N3	C84	1	2	SCD1U10V2KX-4GP	(78.10421.2FL)	DDSP_B_TX_DP_3.C

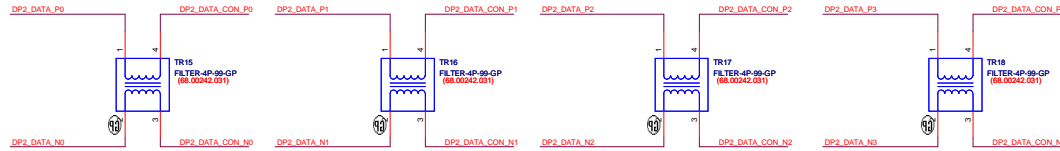
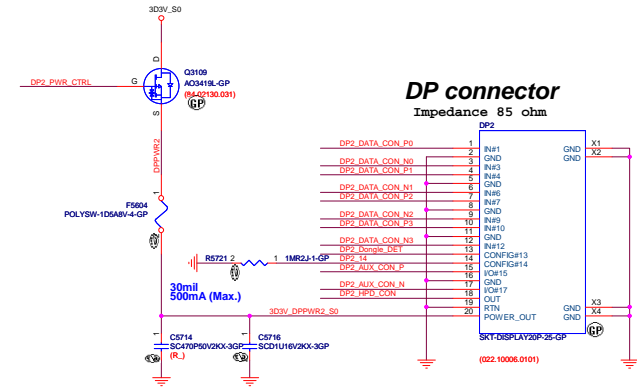
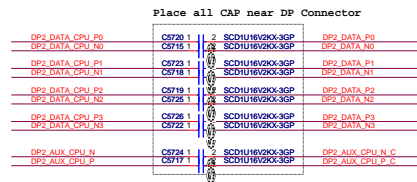


ESD circuit

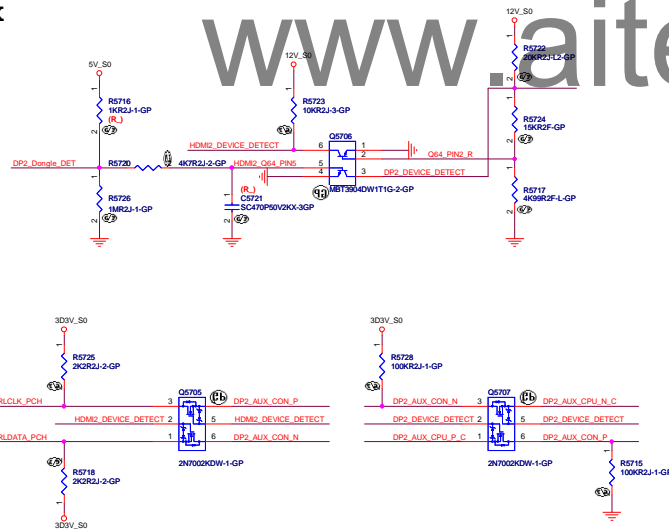


<Core Design>

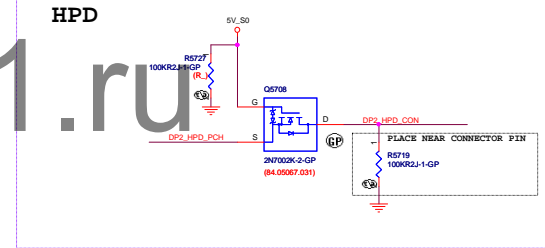
7 DP2_DATA_CPU_P0 <<>
7 DP2_DATA_CPU_N0 <<>
7 DP2_DATA_CPU_P1 <<>
7 DP2_DATA_CPU_N1 <<>
7 DP2_DATA_CPU_P2 <<>
7 DP2_DATA_CPU_N2 <<>
7 DP2_DATA_CPU_P3 <<>
7 DP2_DATA_CPU_N3 <<>
7 DP2_AUX_CPU_N <<>
7 DP2_AUX_CPU_P <<>
16 DP2_CTRLCLK_PCH <<>
16 DP2_CTRLDATA_PCH <<>
16 DP2_HP0_PCH <<>
24 DP2_PWR_CTRL <<>



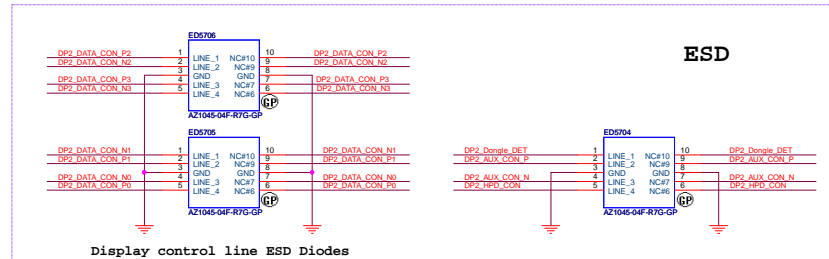
AUX



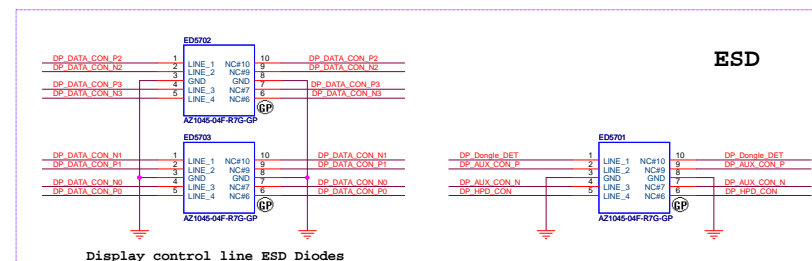
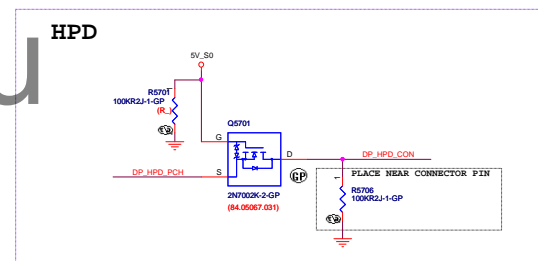
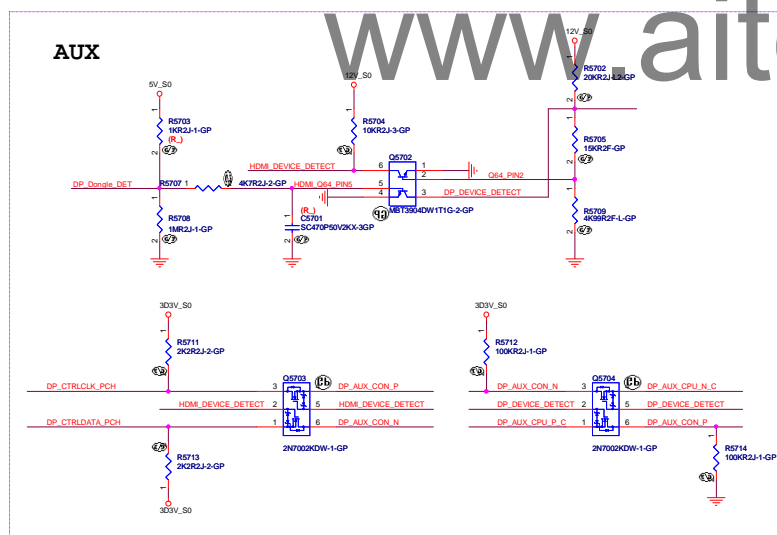
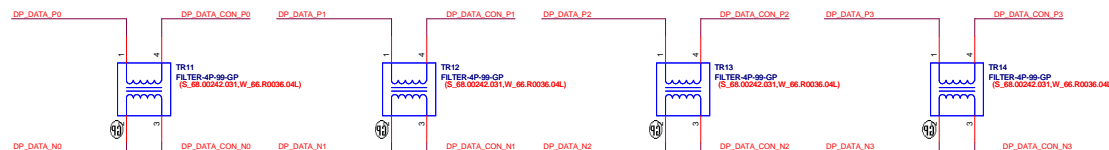
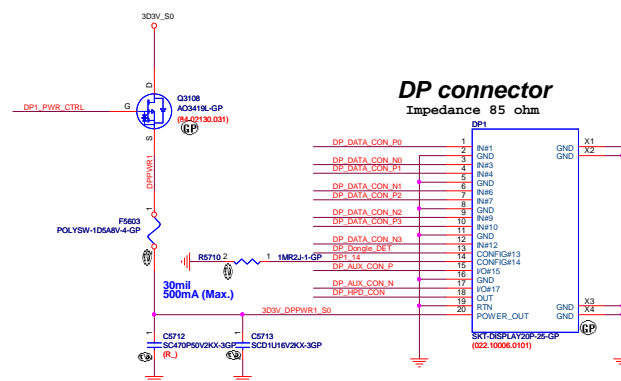
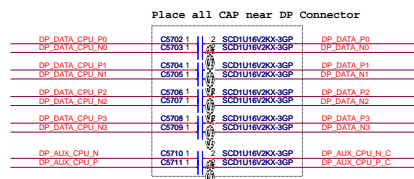
HPD



ESD



<Core Design>

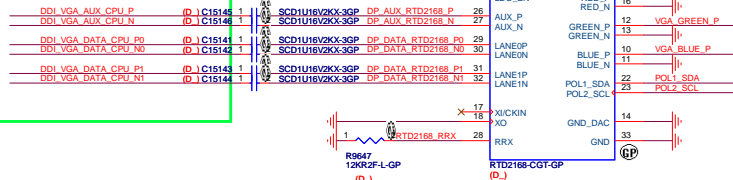


COMPRESSED IMAGE

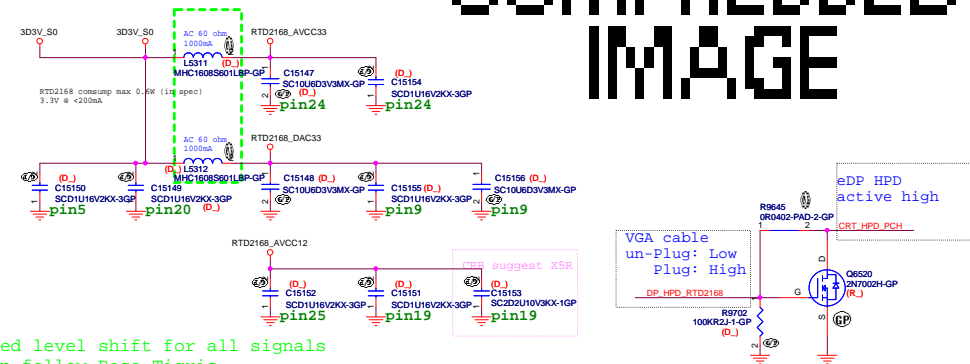
7 DDI_VGA_AUX_CPU_P <<>
7 DDI_VGA_AUX_CPU_N <<>
7 DDI_VGA_DATA_CPU_P0 <<>
7 DDI_VGA_DATA_CPU_N0 <<>
7 DDI_VGA_DATA_CPU_P1 <<>
7 DDI_VGA_DATA_CPU_N1 <<>
16 CRT_HPD_PCH <<>
24 RTD2168_SMBUS_ON <<>
24.64 SIO_CLK <<>
24.64 SIO_DAT <<>

DP to VGA converter: RTD2168

DDI EDP set DP INPUT by VBIOS



@. Check if need level shift for all signals
@. ESD solution follow Rosa Tigris



Mode Configure Table(Power On Latch)

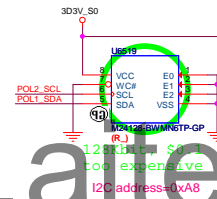
	POL1_SDA(PIN22)	
	0	1
POL2_SCL(PIN23)	0	X
	1	ROM ONLY MODE
		EEPROM MODE



EEPROM MODE

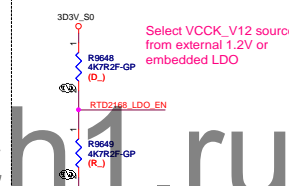
In EEPROM mode, an additional EEPROM is needed. EEPROM should configure with following conditions.

- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8



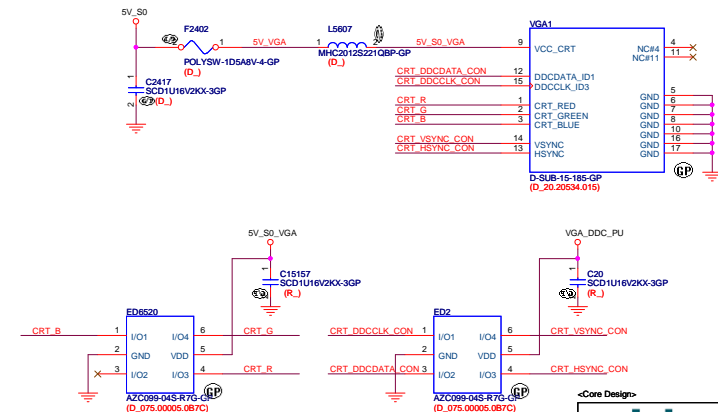
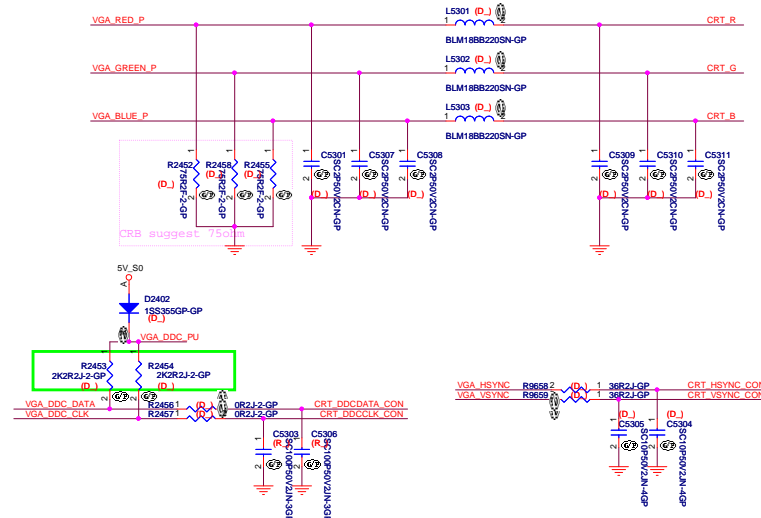
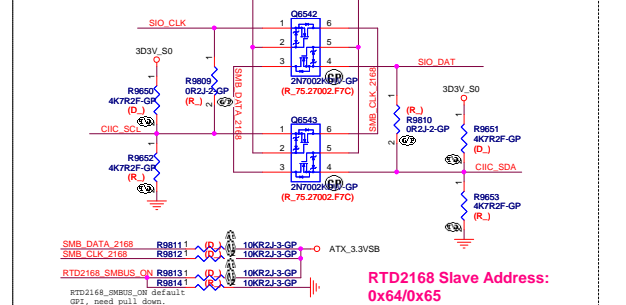
Embedded LDO

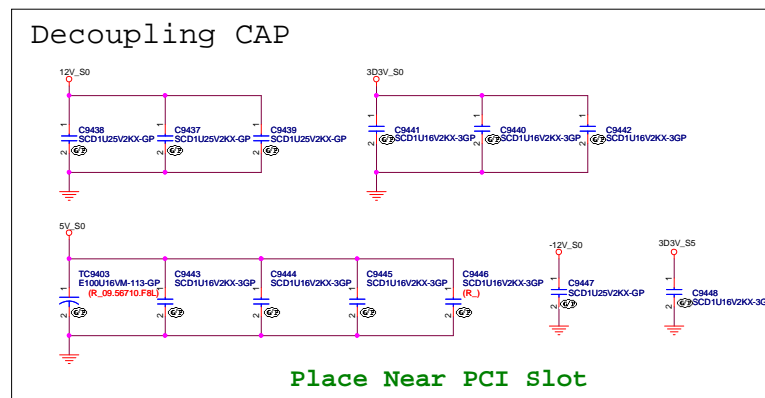
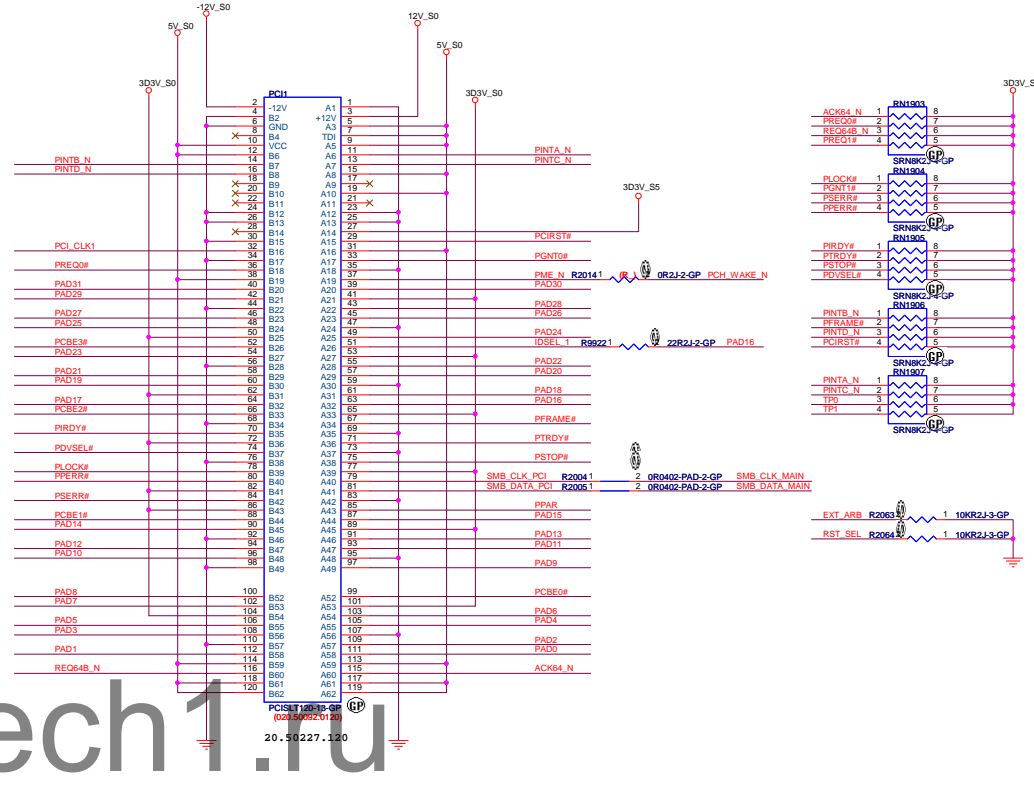
LDO_EN(PIN21)	
0	1
VCC_V12 from External 1.2V	VCC_V12 from Embedded LDO



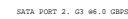
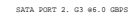
EP Mode

Pin2, Pin3 should be connected to EC for EP mode I2C protocol is used





17	SATA_TX_PCH.N0	>>
17	SATA_TX_PCH.P0	>>
17	SATA_RX_PCH.N0	>>
17	SATA_RX_PCH.P0	>>
17	SATA_TX_PCH.N1	>>
17	SATA_TX_PCH.P1	>>
17	SATA_RX_PCH.N1	>>
17	SATA_RX_PCH.P1	>>
17	SATA_TX_PCH.N2	>>
17	SATA_TX_PCH.P2	>>
17	SATA_RX_PCH.N2	>>
17	SATA_RX_PCH.P2	>>
17	SATA_TX_PCH.N3	>>
17	SATA_TX_PCH.P3	>>
17	SATA_RX_PCH.N3	>>
17	SATA_RX_PCH.P3	>>
17	SATA_TX_PCH.N4	>>
17	SATA_TX_PCH.P4	>>
17	SATA_RX_PCH.N4	>>
17	SATA_RX_PCH.P4	>>
17	SATA_TX_PCH.N5	>>
17	SATA_TX_PCH.P5	>>
17	SATA_RX_PCH.N5	>>
17	SATA_RX_PCH.P5	>>
17	SATAEX_DET0	>>
17	SATAEX_DET1	>>
24	PLT_SATAEX_RST0	>>
19	SATAEX_DEVS0	>>
19	CLK_REG_SEQ_SATA	>>

[illegible]

USB

16 USB_PCH_PP12<<<>>>
16 USB_PCH_PN12<<<>>>

PCIEX1

16 PCIE_RX_PCH_N6<<<>>>
16 PCIE_RX_PCH_P6<<<>>>
16 PCIE_TX_CON_N6<<<>>>
16 PCIE_TX_CON_P6<<<>>>

18 PEG_CLK1_WLAN<<<>>>
18 PEG_CLK1_WLAN#<<<>>>

OTHERS

20,59,63,93,94 PCH_WAKE_N<<<>>>
24,61,63 PLT_WLAN_RST#<<<>>>

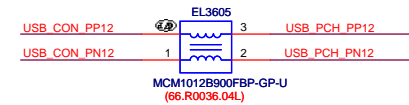
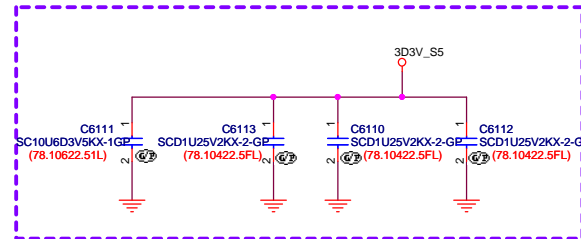
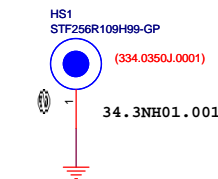
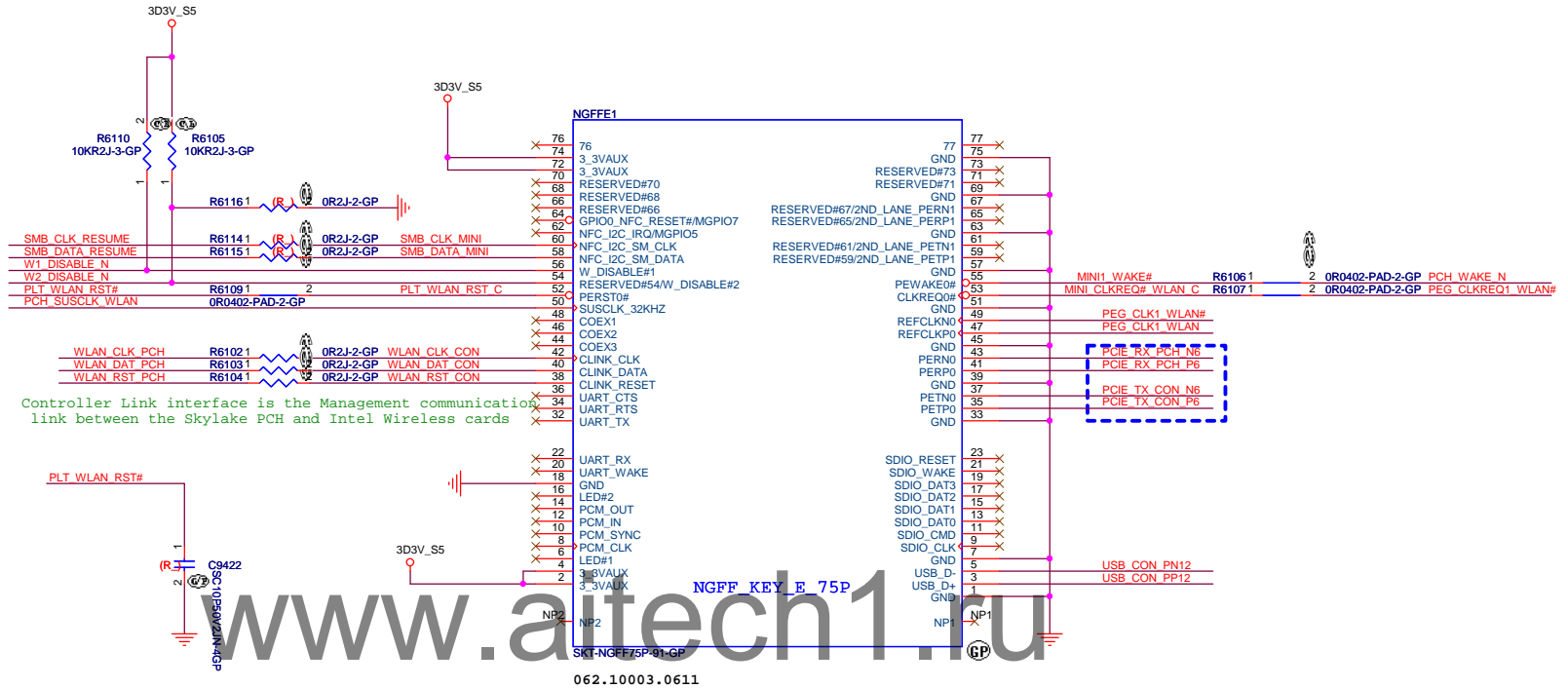
18 PEG_CLKREQ1_WLAN#<<<>>>

17 WLAN_RST_PCH<<<>>>
17 WLAN_DAT_PCH<<<>>>
17 WLAN_CLK_PCH<<<>>>

20 SMB_CLK_RESUME<<<>>>
20 SMB_DATA_RESUME<<<>>>

15 W1_DISABLE_N<<<>>>
15 W2_DISABLE_N<<<>>>
24,61,63 PLT_WLAN_RST#<<<>>>
20 PCH_SUSCLK_WLAN<<<>>>

M.2 2230 / 1630 Key E Type



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien


Title
Mini card-WLAN

Size Document Number
Customer **vHulk**

Date: Wednesday, September 23, 2015 Sheet 61 of 107

Rev
-1

www.aitech1.ru

<Core Design>	
	
Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Haichih, Taipei Hsien	
Title	
Mini card-SSD_(R)	
Size	Document Number
C	vHulk
Date:	Wednesday, September 23, 2015
Sheet	62 of 107
Rev	-1

20 SUSCLK_PCH_M2 >>>

20,59,61,93,94 PCH_WAKE_N <<<
18 PEG_CLKREQ0_M2# <<<
18 PLT_WLAN_RST# <<<

19 SSD_SATA_DEVSUP >>>

17 M2_SATA_DET_PCH <<<

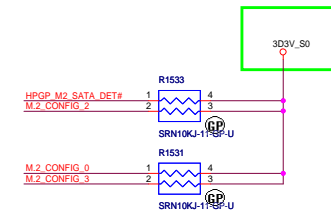
18 PEG_CLK0_M2 <<<
18 PEG_CLK0_M2# <<<

17 SATA_TX_PCH_P2 <<<
17 SATA_TX_PCH_N2 <<<

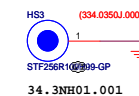
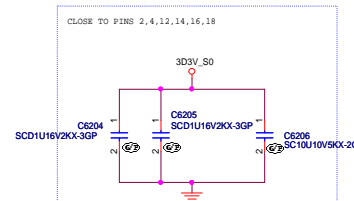
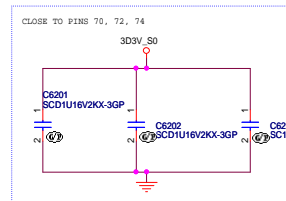
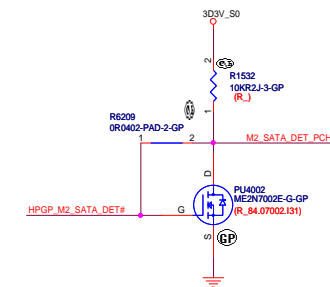
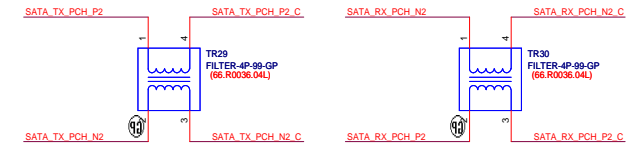
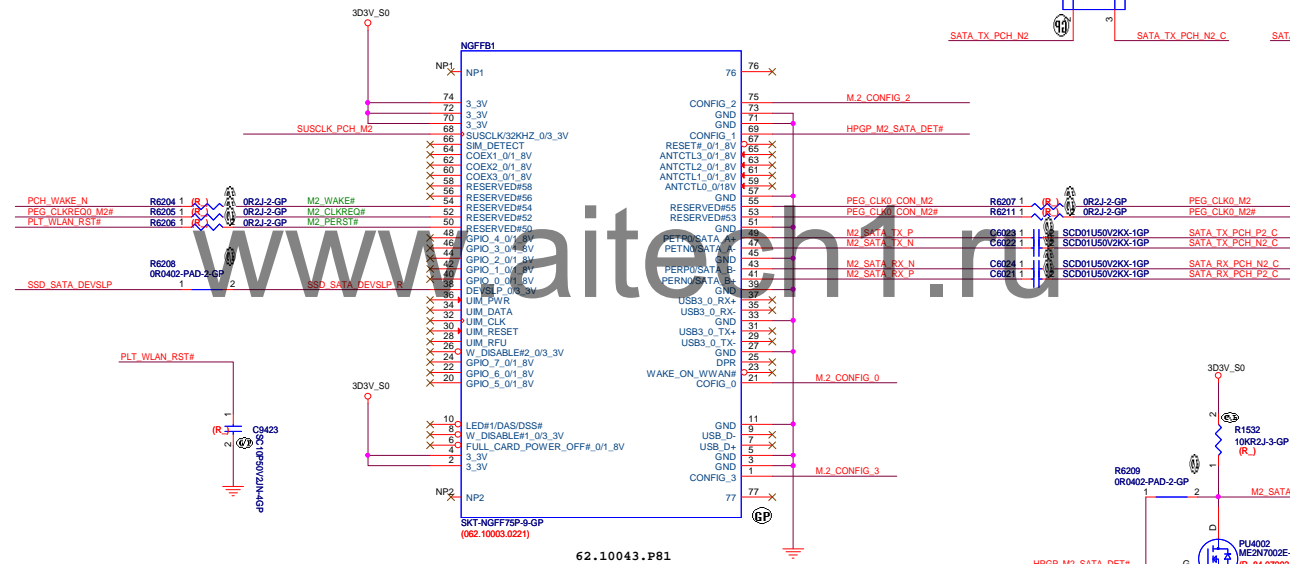
17 SATA_RX_PCH_P2 <<<
17 SATA_RX_PCH_N2 <<<

Table 46. Socket 2 Module Configuration Table

Module Configuration Decodes				Module Type and Main Host Interface ¹	Port Configuration ²
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN - PCIe	0



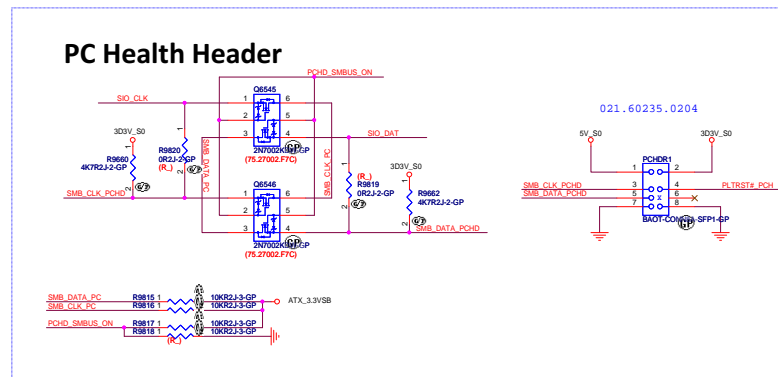
M.2 Key B Type



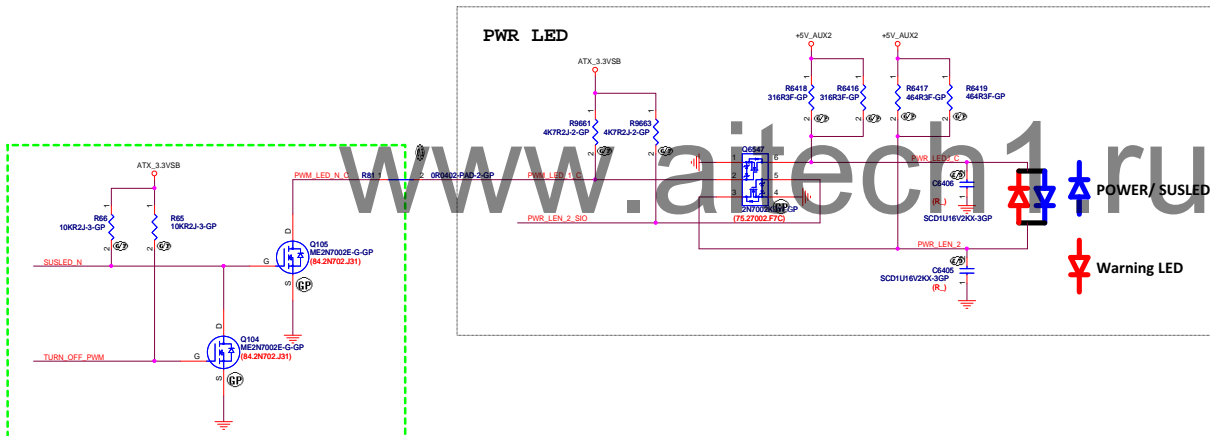
FRONT PANEL HEADER

21. 62738. 207

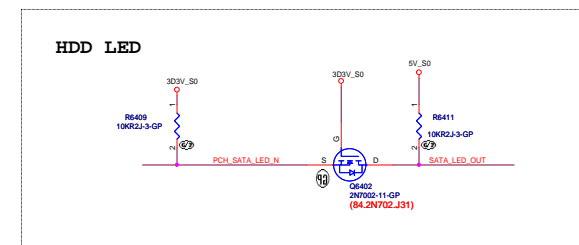
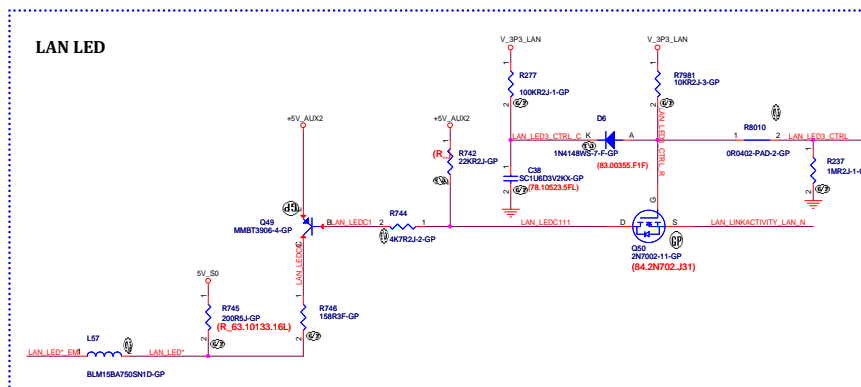
5V_S0
RS402 10KSP-GP
LEDH1
SATA_LED_PWR
FP_RST_N
+5V_AUX2
TOR-CONTR-SFP-GP-U
ATX_3.3V/5B
RS403 10KSP-3-GP
RS404 1
33R02-3-GP
PHY88TN_2H
CA402 SC11U0V2KX-1GP
CA401 SC1K1P50V2KX-1GP

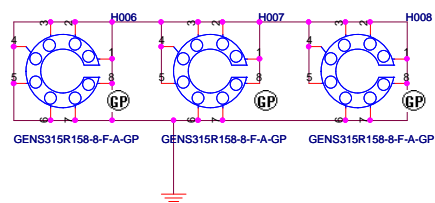
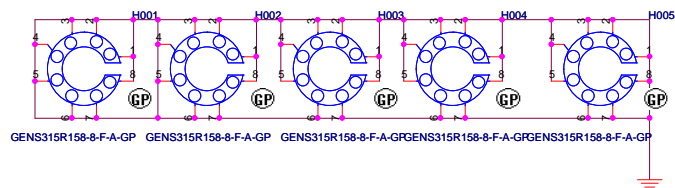


	S0	S0 / Warning	S3	S3 / Warning	S4	S5
SUSLED_N	HIGH	LOW	H & L Circling (Blink)	LOW	HIGH	LOW
PWR_LEN_2_SIO	HIGH	H & L Circling (Blink)	HIGH	H & L Circling (Blink)	LOW	HIGH



System State/Health	Indicator Behavior
S0/ Good 	Blue
S0/ Warning or 	Blink Red
S3/ Good 	Blink Blue
S3/ Warning or 	Blink Red
S4	No light
S5	No light





LABEL



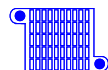
LBL1 W30*H15
(40.3BZ24.011)

Battery Symbol



BAT1 BATTERY CR2032 (23.20068.001)
23.20068.001 KTS BBBCR2032BX
23.20023.311 MITSUBISHI CR2032 MITSUBISHI
23.22063.001 JHT CR2032 JHT

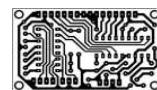
HeatSink Symbol



PCHHS1 HEATSINK (60.3ET05.001)

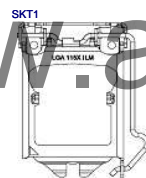
Vendor P/N:
60.3ET05.001
60.3ET05.021

PCB Symbol



PCB (348.02802.0011)

SKYLake SOCKET



Load Plate (22.78006.001)

Vendor: FOXCONN
P/N: 22.78006.001

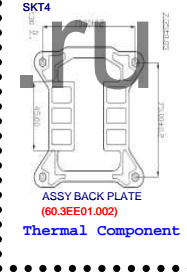
Vendor: LOTES
P/N: 22.78005.181



Back Plate (22.78006.011)

Vendor: FOXCONN
P/N: 22.78006.011
Thickness: 2.0mm (with mylar)

Vendor: LOTES
P/N: 022.70001.0121
Thickness: max 2.2mm (with mylar)



ASSY BACK PLATE (60.3EE01.002)
Thermal Component



ILMCOVER (22.78005.281)

Vendor: FOXCONN
P/N: 22.78005.281

Vendor: LOTES
P/N: 22.78005.171

<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title		Others
Size	Document Number	Rev
Customer	YHulk	-1
Date:	Wednesday, September 23, 2015	Sheet 65 of 107

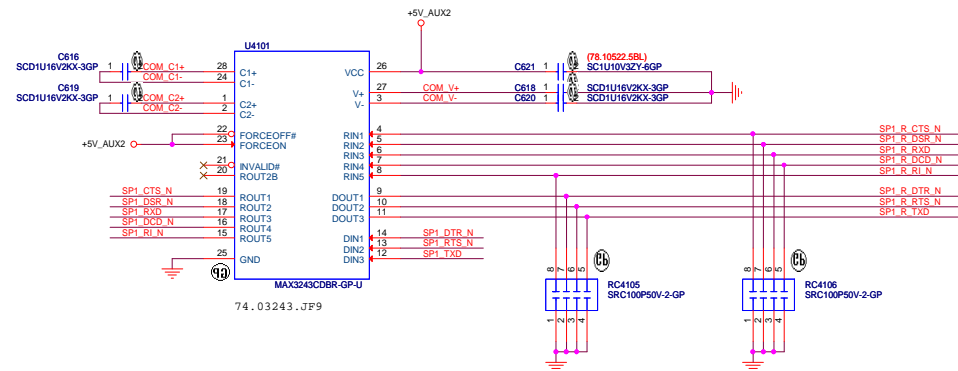
www(R)aitech1.ru

<Core Design>		wistron		Wistron Incorporated	
				21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title					
IO Board_(R)					
Size	Document Number				Rev
C	vHulk				-1
Date:	Wednesday, September 23, 2015		Sheet	66	of 107

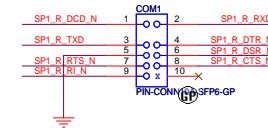
COM1



SERIAL PORT



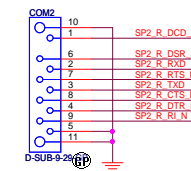
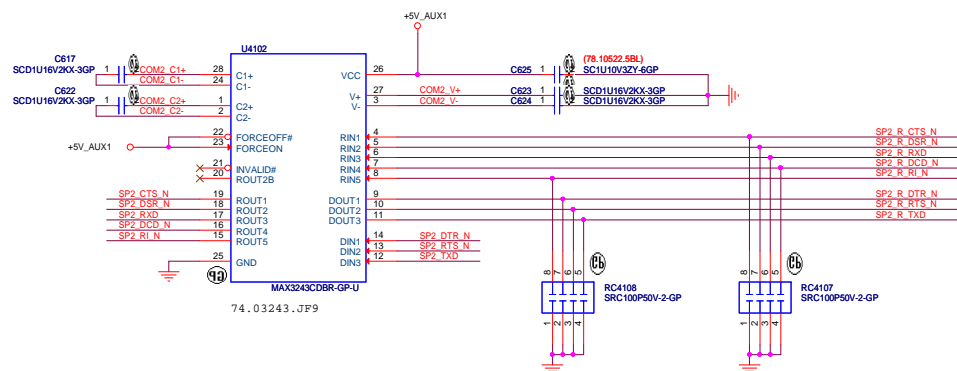
COM port header



COM2



SERIAL PORT



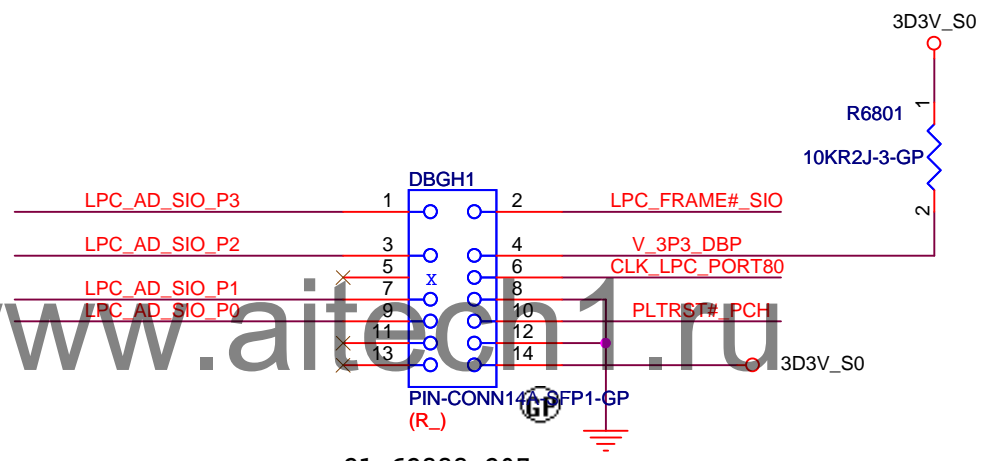
19,24,91 LPC_AD_SIO_P3 << >>
19,24,91 LPC_AD_SIO_P2 << >>
19,24,91 LPC_AD_SIO_P1 << >>
19,24,91 LPC_AD_SIO_P0 << >>

19,24,91 LPC_FRAME#_SIO << >>

19,91 CLK_LPC_PORT80 << >>
15,24,64,91,97 PLTRST#_PCH << >>

80 port


Layout close to SIO



21.62888.207

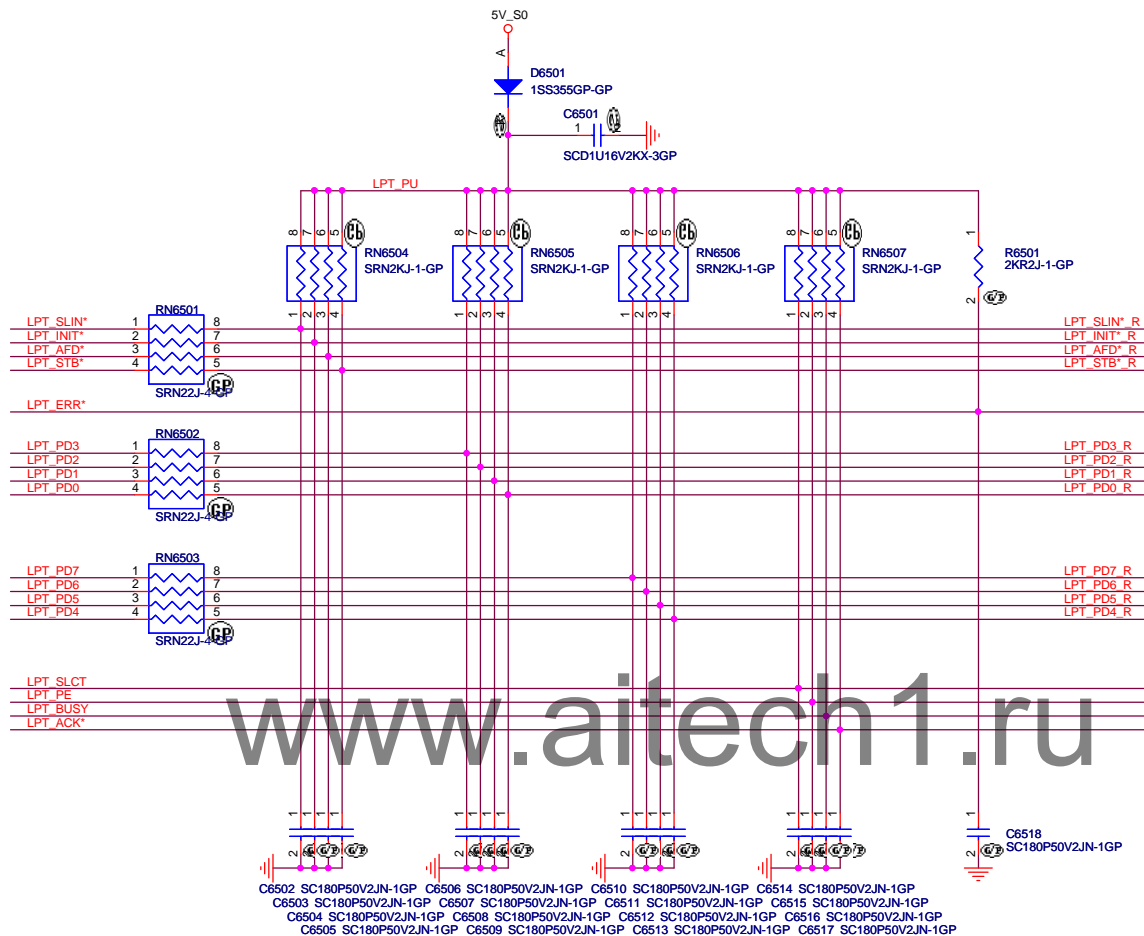
Annie pin define

<Core Design>

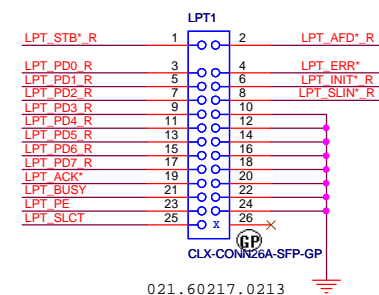
		Wistron Incorporated 21F, 88, Sec.1,Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title Debug			
Size Custom	Document Number vHulk		Rev -1
Date:	Wednesday, September 23, 2015	Sheet	68 of 107

PARALLEL PORT

24 LPT_SLCT
24 LPT_PE
24 LPT_BUSY
24 LPT_ACK*
24 LPT_SLIN*
24 LPT_ERR*
24 LPT_AFD*
24 LPT_STB*
24 LPT_INIT*
24 LPT_PD[7:0] <<



LPT




<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien


Title	LPT	
Size	Document Number	Rev
Custom	vHulk	-1
Date:	Wednesday, September 23, 2015	Sheet 69 of 107

www.altech1.ru


<Core Design>	
 Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Haichih, Taipei Hsien	
Title	
G sensor_(R)	
Size C	Document Number vHulk
Date: Wednesday, September 23, 2015	Sheet 70 of 107
Rev -1	

(R)
www.aitech1.ru

(R)
www.aitech1.ru


<Core Design>	
 Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title Thunderbolt (R)	
Size C	Document Number vHulk
Date: Wednesday, September 23, 2015	Rev -1
Sheet 72 of 107	

(R)
www.aitech1.ru

<Core Design>			
		Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title			
Thunderbolt (R)			
Size	Document Number	Rev	
C	vHulk	-1	
Date:	Wednesday, September 23, 2015	Sheet	73 of 107

(R)
www.aitech1.ru

(R)
www.aitech1.ru

<Core Design>	
 Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Haichih, Taipei Hsien	
Title Thunderbolt (R)	
Size C	Document Number vHulk
Date: Wednesday, September 23, 2015	Rev -1
Sheet 75 of 107	

(R)
www.aitech1.ru

(R)
www.aitech1.ru

(R)
www.aitech1.ru

(R)
www.aitech1.ru

(R)
www.aitech1.ru

(R)
www.aitech1.ru

(R)
www.aitech1.ru


(R)
www.aitech1.ru

(R)
www.aitech1.ru

(R)
www.aitech1.ru

(R)
www.aitech1.ru

(R)
www.aitech1.ru

<Core Design>			
		Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Haichih, Taipei Hsien	
Title			
GPU Switch_(R)			
Size	Document Number		Rev
C	vHulk		-1
Date:	Wednesday, September 23, 2015	Sheet	87 of 107

(R)
www.aitech1.ru

(R)
www.aitech1.ru

(R)
www.aitech1.ru

<Core Design>		wistron		Wistron Incorporated	
				21F, 88, Sec.1,Hsin Tai Wu Rd Haichih, Taipei Hsien	
Title					
NFC_(R)					
Size	Document Number				Rev
C	vHulk				-1
Date:	Wednesday, September 23, 2015		Sheet	90	of 107

19,24,68 LPC_FRAME#_SIO <<>> LPC_FRAME#

19,68 CLK_LPC_PORT80 <<>> CLK_PCI_LPC

15,24,64,68,97 PLTRST#_PCH <<>> PLTRST#_PCH

19,24,68 LPC_AD_SIO_P3 <<>> LPC_AD3

19,24,68 LPC_AD_SIO_P2 <<>> LPC_AD2

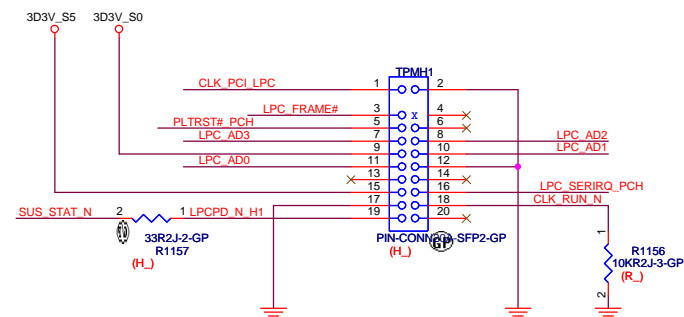
19,24,68 LPC_AD_SIO_P1 <<>> LPC_AD1

19,24,68 LPC_AD_SIO_P0 <<>> LPC_AD0

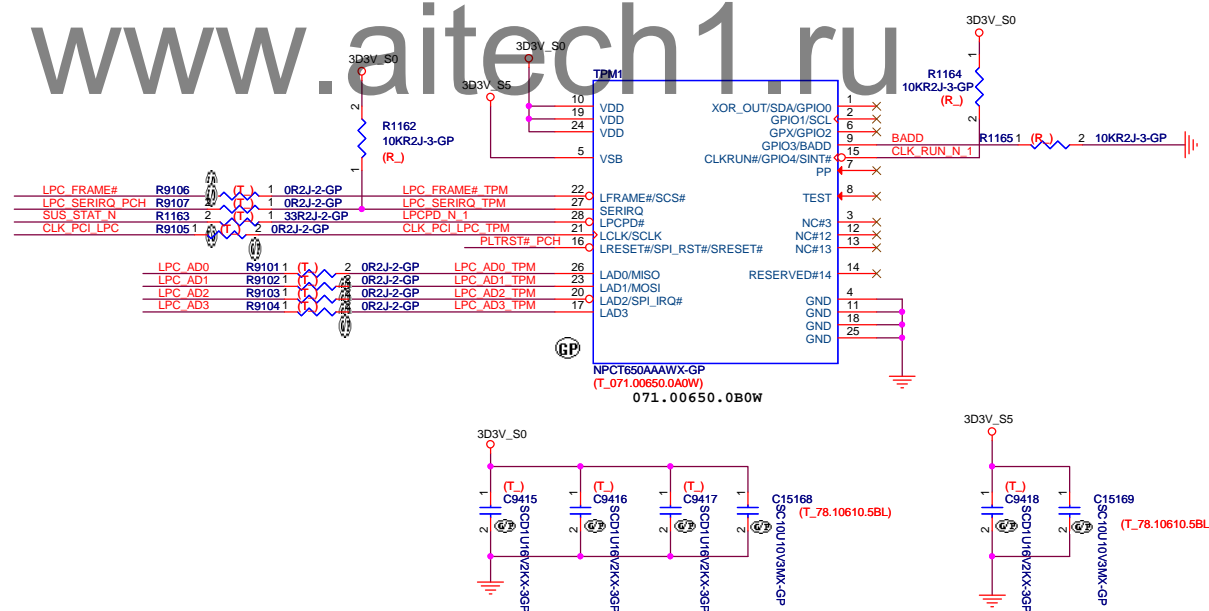
19 SUS_STAT_N <<>>

19,24 LPC_SERIRQ_PCH <<>>

TPM 2.54 pitch Header



TPM onboard chip for Q170



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

File

TPM

Size

Document Number

Customer

vHulk

Rev

-1

Date:

Wednesday, September 23, 2015

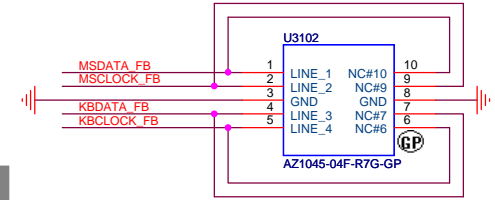
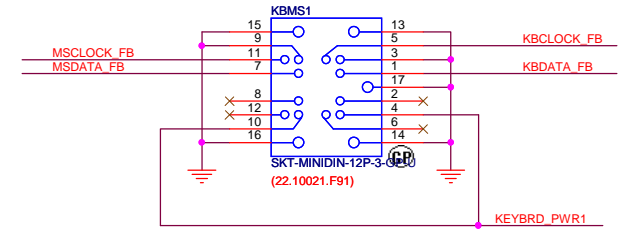
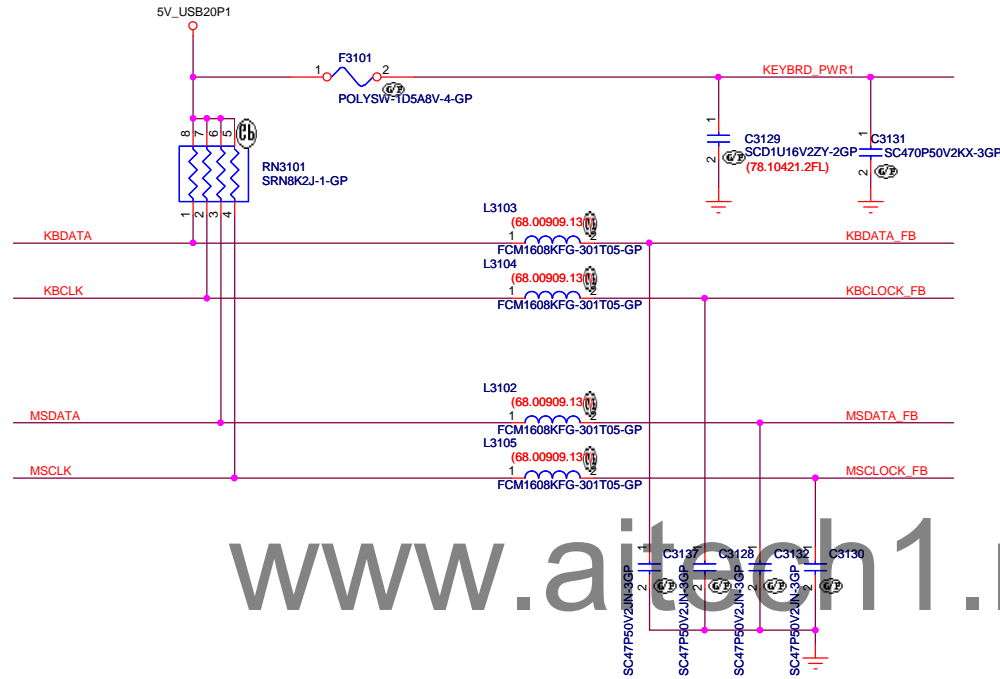
Sheet

91

of

107

24 KBDATA
24 KBCLK
24 MSDATA
24 MSCLK



<Core Design>

wistron

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title

PS2

Size

Document Number

Custom

vHulk

Rev

-1

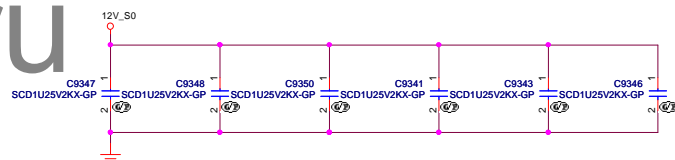
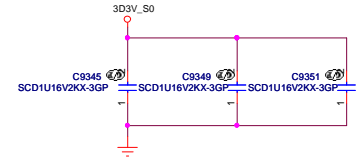
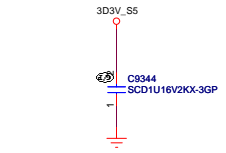
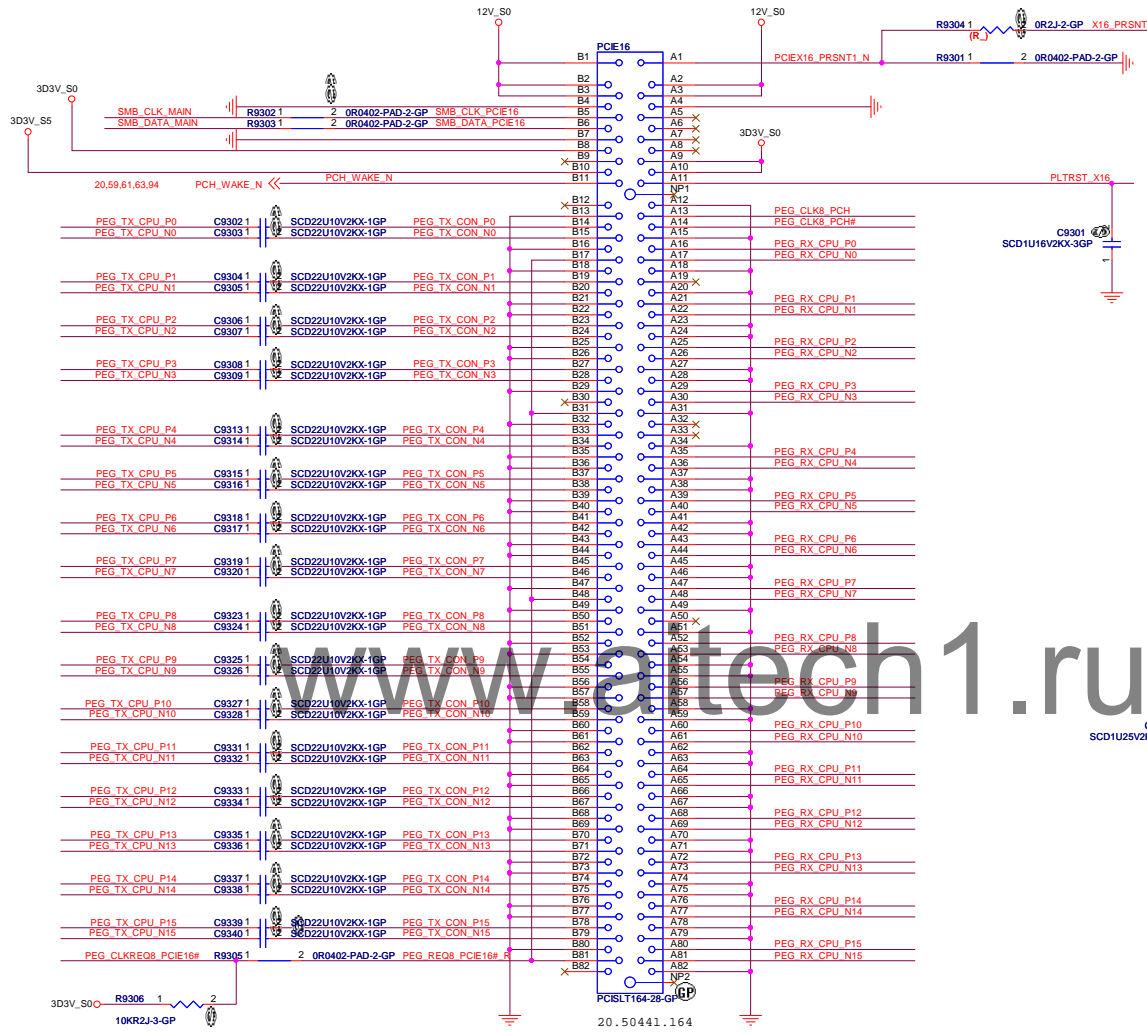
Date:

Wednesday, September 23, 2015

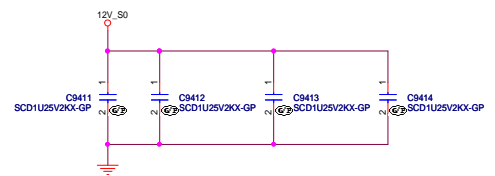
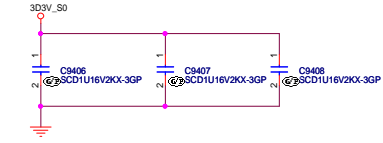
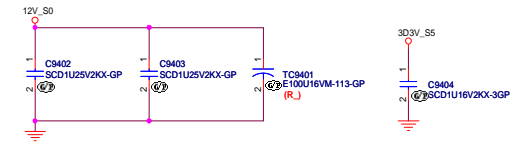
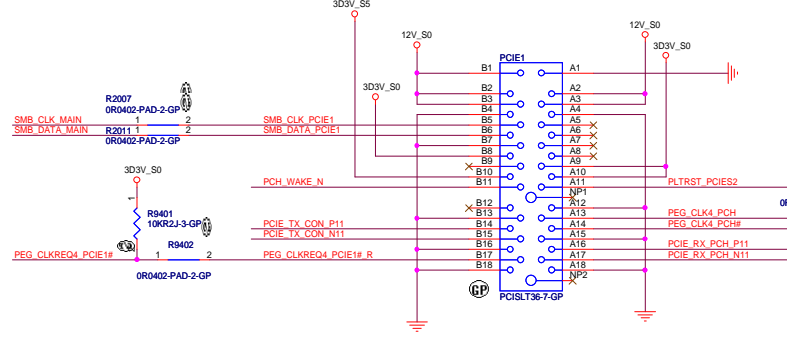
Sheet

92 of 107

3 PEG_TX_CPU_P0[0..15] >>>
3 PEG_TX_CPU_N0[0..15] >>>
11,12,13,14,20,59,94 SMB_CLK_MAIN >>>
11,12,13,14,20,59,94 SMB_DATA_MAIN >>>
18 PEG_CLK8_PCH >>>
18 PEG_CLK8_PCH# >>>
15 X16_PRSNT <<<
24 PLTRST_X16 >>>
18 PEG_CLKREQ8_PCIE16# <<<

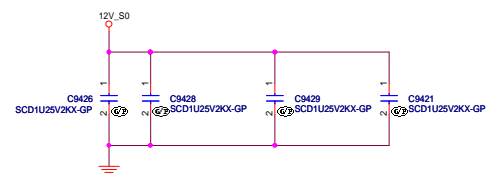
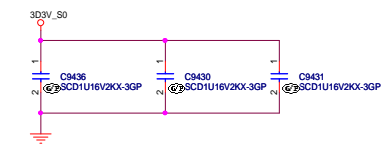
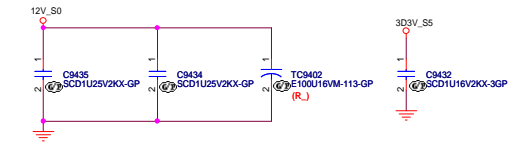
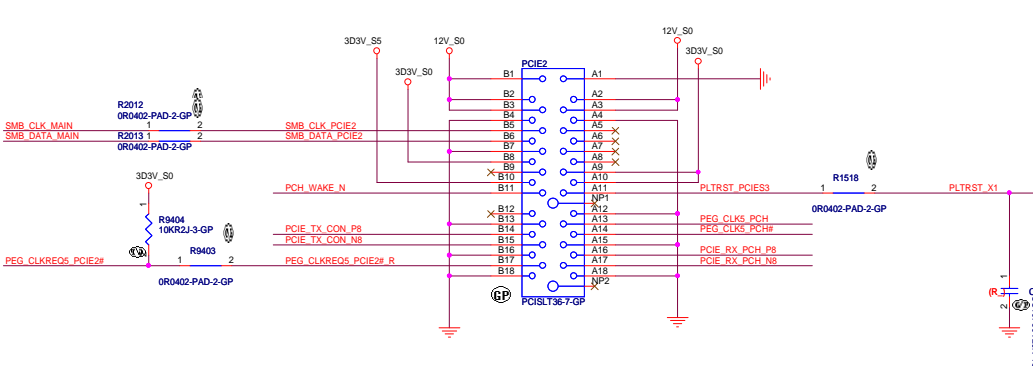


PCIEX1 CONN



www.aitech1.ru

PCIEX1 CONN



(R)
www.aitech1.ru

www.(R)itech1.ru

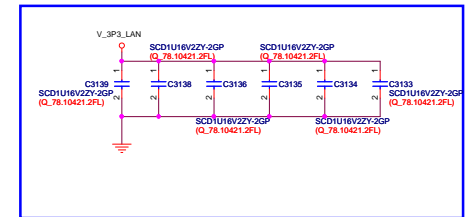
31,32	LAN_MDI_LAN_P0	»»
31,32	LAN_MDI_LAN_N0	
31,32	LAN_MDI_LAN_P1	»»
31,32	LAN_MDI_LAN_N1	
31,32	LAN_MDI_LAN_P2	»»
31,32	LAN_MDI_LAN_N2	
31,32	LAN_MDI_LAN_P3	»»
31,32	LAN_MDI_LAN_N3	
32,97	LAN_SPEED1000_LAN_N	»»
32,97	LAN_SPEED100_LAN_N	
.97	LAN_LINKACTIVITY_LAN_N	»»
24	LAN_EN_PWR_SIO	»»

V_3P3_LAN

CA628
SC220ED3V5MX-2GP
(Q_)

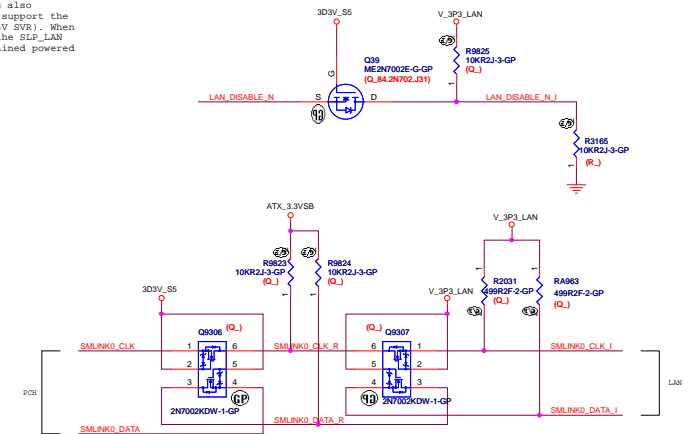
CA575
SCD1U16V2ZY-2
(Q_78.10421.2)

Place near Pin5




Internal SRV	Shared with PCH's 1.05V SVR
LA36 : STUFF	LA36 : NO STUFF
RA1020 : NO STUFF	RA1020 : STUFF
R968 : STUFF	R968 : NO STUFF
RA886 : NO STUFF	RA886 : STUFF

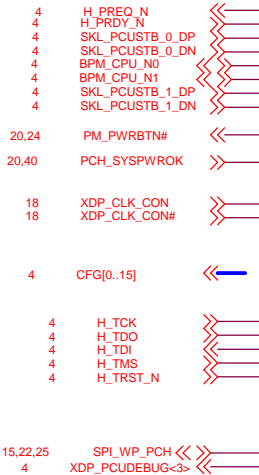
10Mb: Green
100Mb: Green
1Gb: Orange
Active: Yellow Light flash



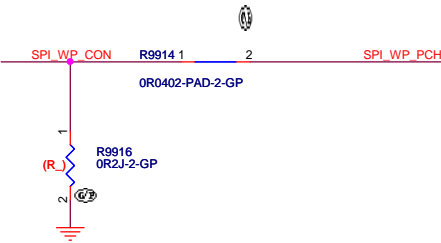
www.altech1.ru

<Core Design>	
 Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Haichih, Taipei Hsien	
Title	
LAN Switch_(R)	
Size	Document Number
C	vHulk
Date:	Wednesday, September 23, 2015
Sheet	98 of 107
Rev	-1

XDP for CPU



XDP for CPU



<Core Design>



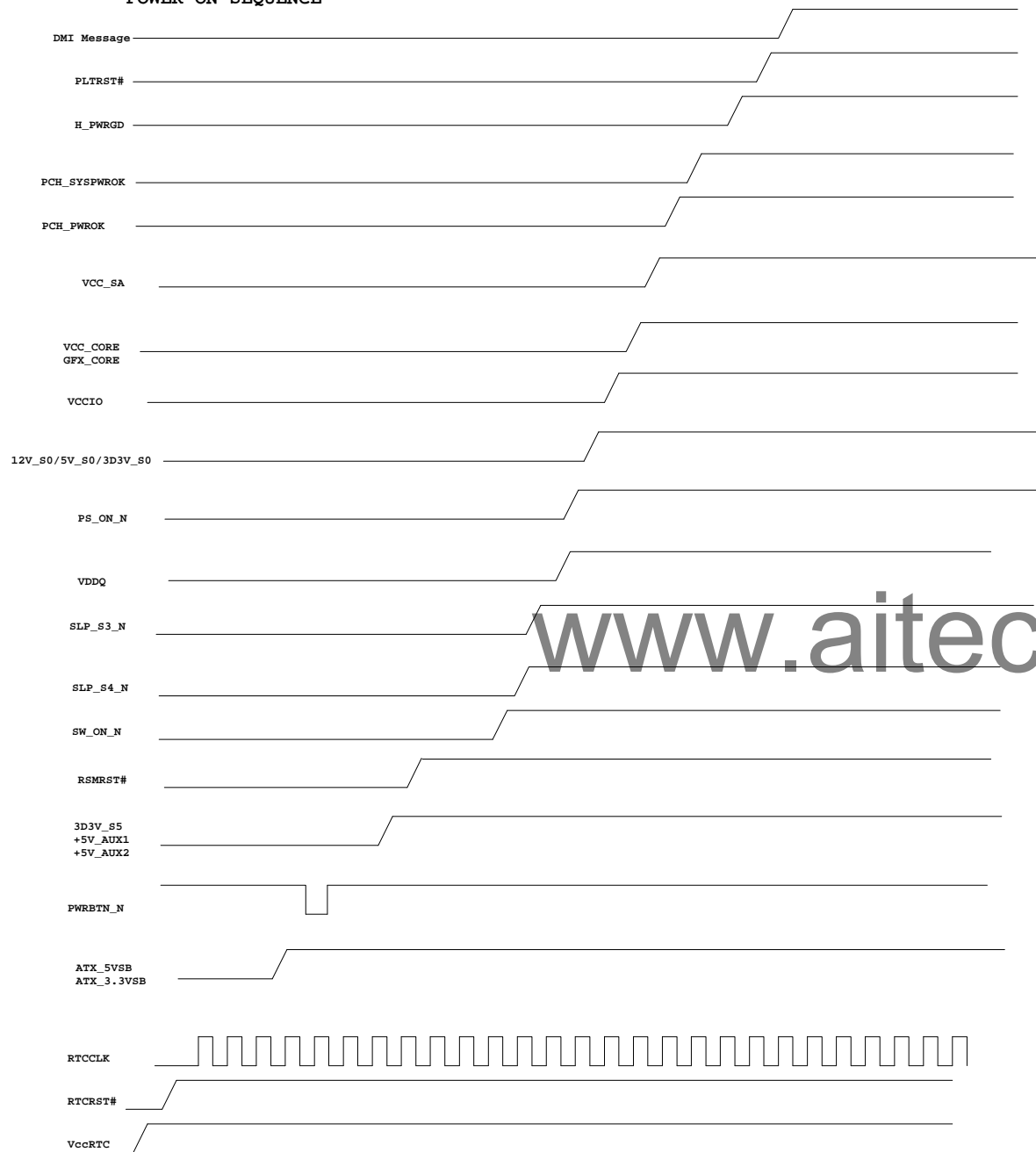
Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

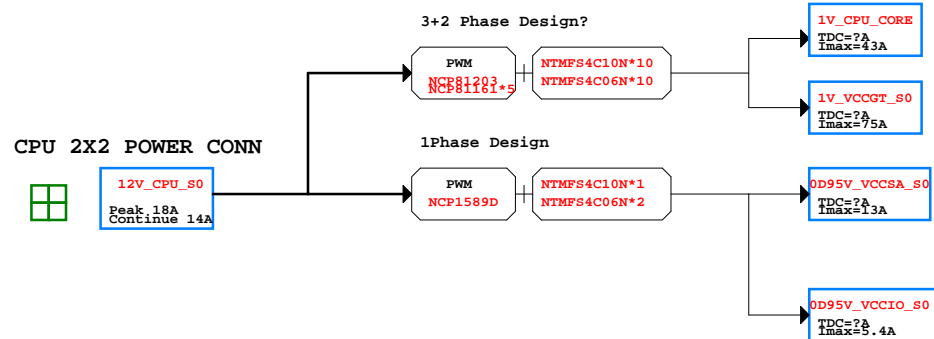
Title			XDP&ITP
Size	Document Number	Rev	
Custom	vHulk	-1	
Date:	Wednesday, September 23, 2015	Sheet	99 of 107

(R)
www.aitech1.ru

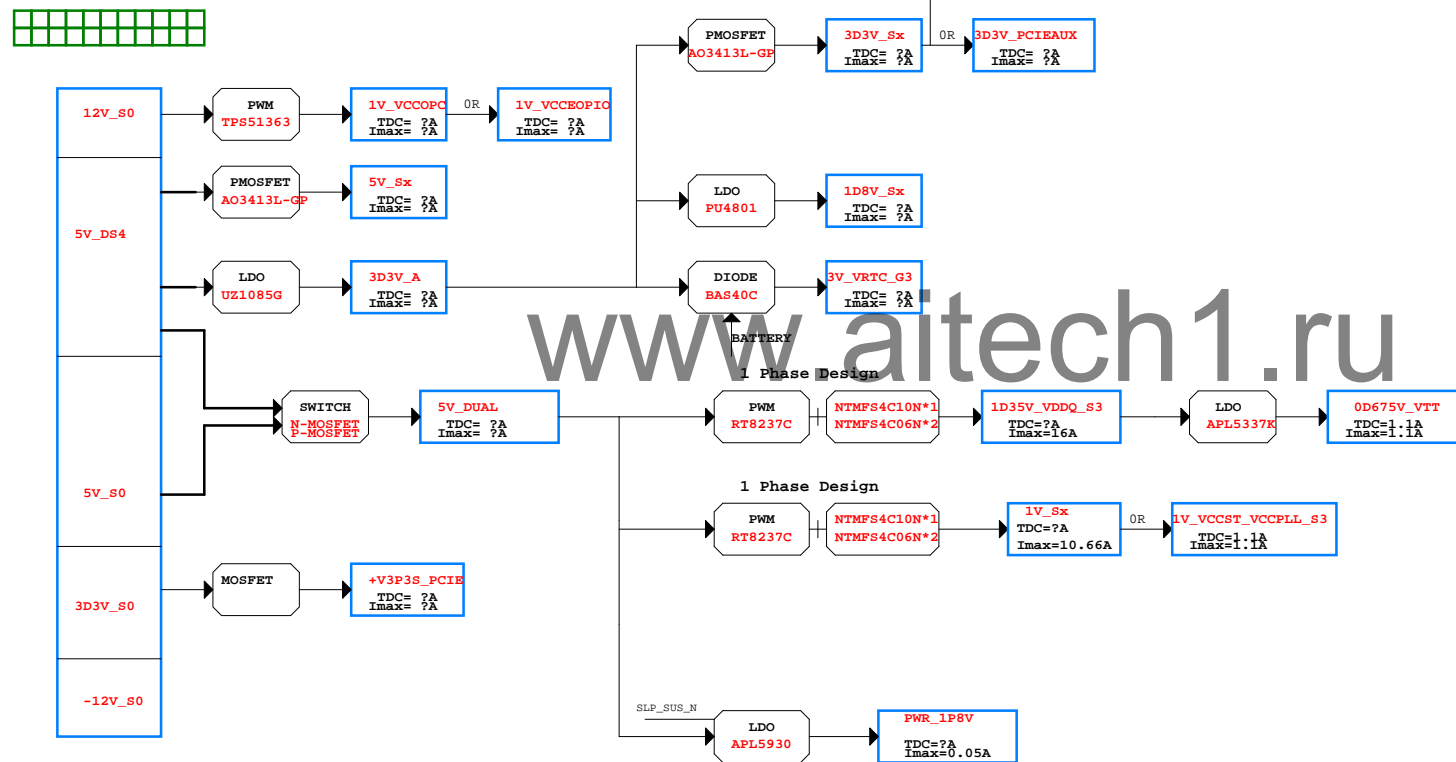
www.aitech1.ru

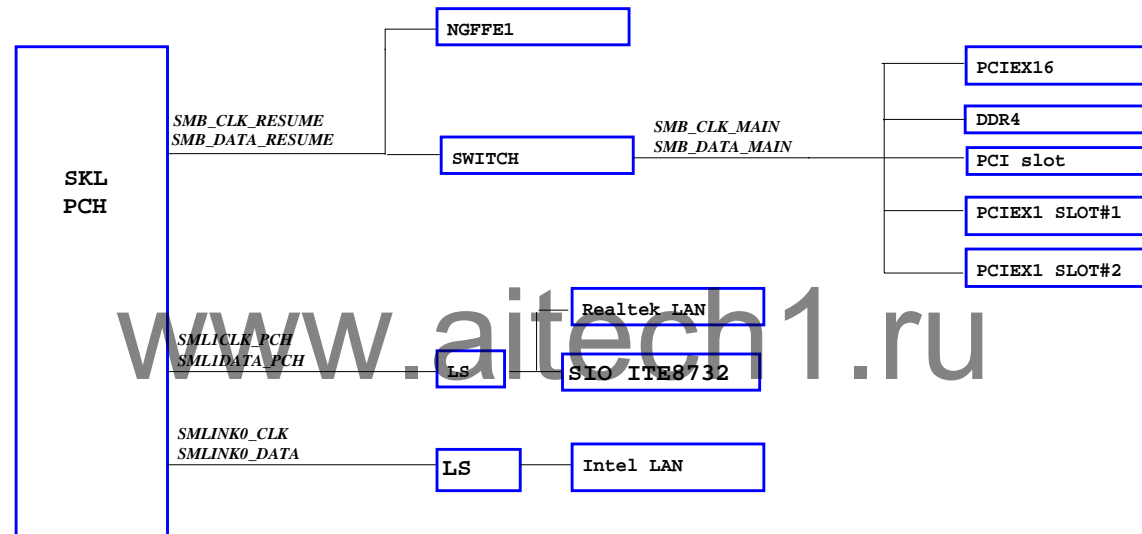
POWER ON SEQUENCE

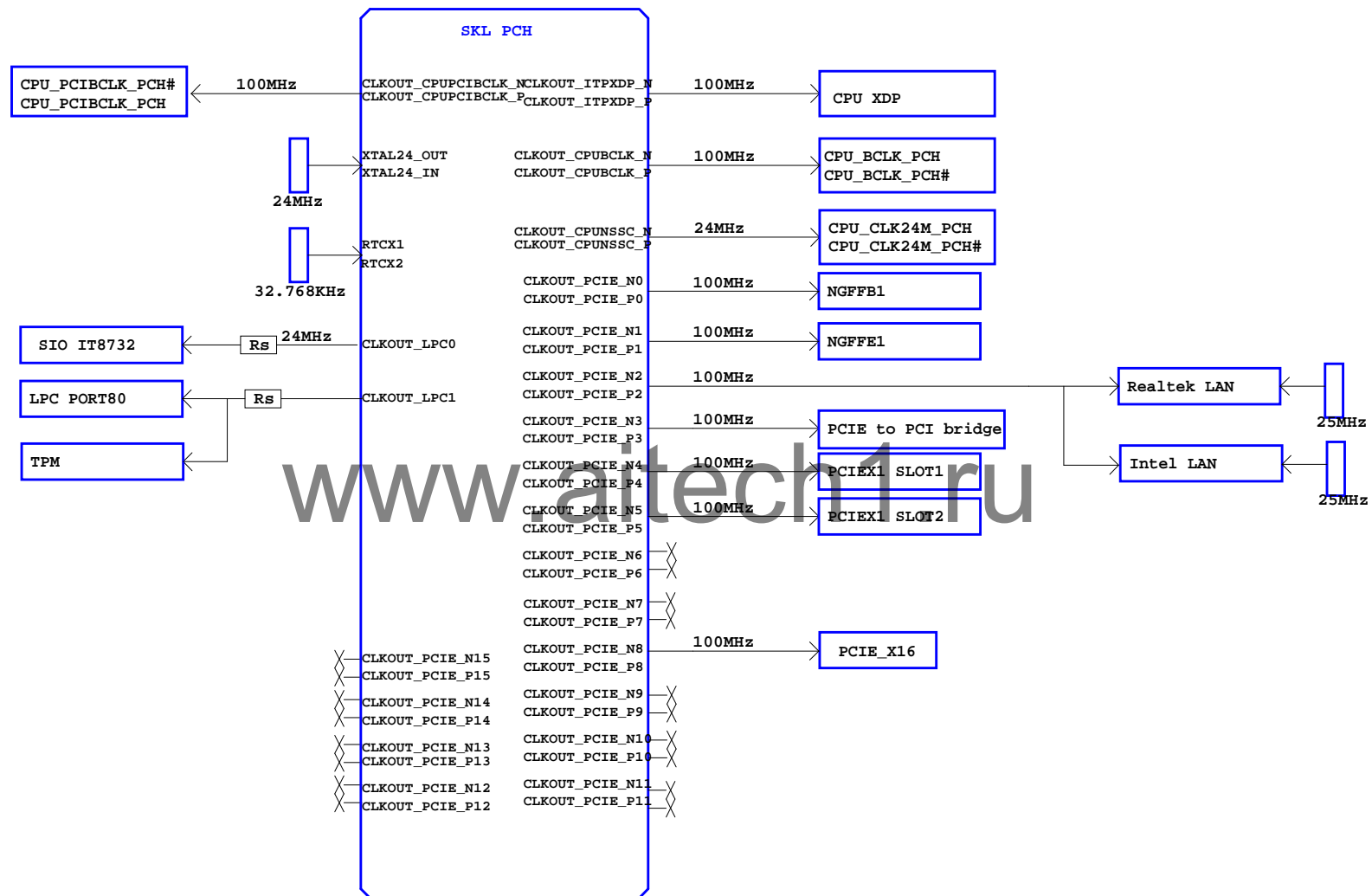


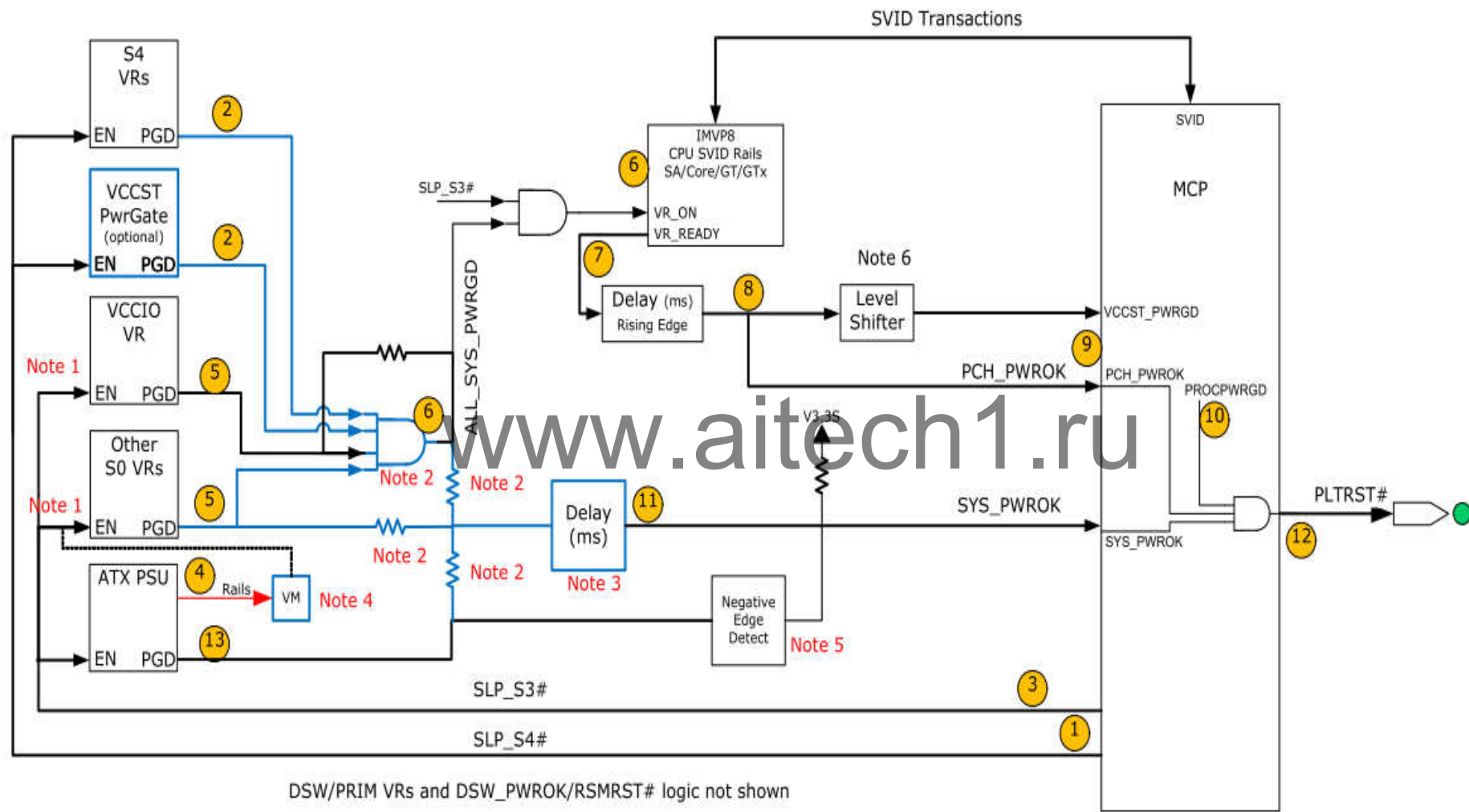


ATX 2X12 POWER CONN










(R)
www.aitech1.ru

<Core Design>				Wistron Incorporated 21F, 88, Sec.1 Hsin Tai Wu Rd Haichih, Taipei Hsien					
Title									
Change History									
Size	Document Number				Rev				
C	vHulk				-1				
Date:	Wednesday, September 23, 2015		Sheet	107	of 107				